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THESIS

FREQUENCY-BASED LOAD SHARING IN CURRENT-MODE-CONTROLLED BUCK CONVERTERS

by

Jonathan E. Moore

March 1999

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REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-

Public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instruction, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Washington Headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302, and to the Office of Management and Budget, Paperwork Reduction Project (0704-0188) Washington DC 20503.

1. AGENCY USE ONLY *(Leave blank)*

2. REPORT DATE
March 1999

3. REPORT TYPE AND DATES COVERED
Master's Thesis

4. TITLE AND SUBTITLE
Frequency-Based Load Sharing in Current-Mode-Controlled Buck Converters

5. FUNDING NUMBERS

6. AUTHOR(S)
Jonathan E. Moore

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
Naval Postgraduate School
Monterey, CA 93943-5000

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

10. SPONSORING / MONITORING AGENCY REPORT NUMBER

11. SUPPLEMENTARY NOTES
The views expressed in this thesis are those of the author and do not reflect the official policy or position of the Department of Defense or the U.S. Government.

12a. DISTRIBUTION / AVAILABILITY STATEMENT
Approved for public release; distribution is unlimited.

12b. DISTRIBUTION CODE

13. ABSTRACT *(maximum 200 words)*

Modular DC Zonal Electrical Distribution (DC ZEDS) offers advantages in both cost and weight over traditional radial shipboard distribution. In order to equip the next class of surface combatant with DC ZEDS, preparative research includes the design of autonomous dc-to-dc power converter modules having robust load sharing capability. This thesis examines the combined utility of current-mode switch control and frequency-based load sharing to promote equal load sharing among parallel dc-to-dc converter modules.

Current-mode control with frequency-based load sharing is analyzed primarily with digital simulation. To that end, a state-space representation for a system of two converters and an Advanced Continuous Simulation Language (ACSL) simulation for a system of three converters are developed. Various studies were conducted to evaluate the performance of a proposed system for load sharing performance between dissimilar converters, for step changes in load, and for bringing a converter off-line . Additionally, a sub-circuit of frequency-based control—the rms frequency estimation circuit—was built, and its static performance evaluated. Finally, recommendations are made for further simulations which will better test the dynamic performance of this rms estimation circuit and the system of parallel converters employing frequency-based load sharing as a whole.

14. SUBJECT TERMS
DC-to-DC Buck Converter, Current-Mode, Frequency-Based Load Sharing, Paralleling, ACSL

15. NUMBER OF PAGES
116

16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT
Unclassified

18. SECURITY CLASSIFICATION OF THIS PAGE
Unclassified

19. SECURITY CLASSIFICATION OF ABSTRACT
Unclassified

20. LIMITATION OF ABSTRACT
UL

NSN 7540-01-280-5500

Standard Form 298 (Rev. 2-89
Prescribed by ANSI Std. 239-18, 298-10

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FREQUENCY-BASED LOAD SHARING IN CURRENT-MODE-CONTROLLED BUCK CONVERTERS

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Lieutenant, United States Navy
B.S., University of Washington, 1991

Submitted in partial fulfillment of the
requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

from the

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I. PROJECT BACKGROUND

A. RADIAL DISTRIBUTION

The standard paradigm for electric power distribution aboard Navy ships is radial distribution. With this scheme, a small number of 60 Hz generators located throughout the ship supply power to all shipboard loads via a hierarchical array of switchboards. The distribution system in any ship is designed to survive reasonably expected battle damage, such as disabling a single generator or large distribution switchgear. Survivability for loads considered vital to the ship's mission is realized by powering them redundantly. Vital loads can be thought of as the merging of branches from hierarchical trees of two separate generators.

Loads in each physical area of the ship are generally powered by local power panels. However those local power panels receive power from many different switchgear located throughout the ship. Many such local power panels will be located within most watertight sections of the ship. Sometimes it is necessary to secure power to a group of loads in close physical proximity, say to isolate a watertight compartment. With radial distribution it becomes very difficult to quickly secure power to them. Further, each class of ship has a different set of vital loads and a different number and location of generators. Thus it is virtually impossible to standardize radial distribution over several classes of ships. Also, radial distribution systems require immense manpower efforts to operate and maintain. For these two reasons, an alternative to radial distribution is sought.

B. ZONAL DISTRIBUTION

An alternative is zonal distribution. With a zonal scheme, two redundant longitudinal buses are fed by each generator. Both buses pass through a number of distribution zones, supplying power to loads within each of those zones. Distribution zones will most logically correspond to flooding control zones divided by primary watertight bulkheads. The strategy for separation of these two main electrical distribution buses will be much the same strategy as for separation of the shipboard firemains—one above and one below the waterline, one port and one starboard, minimizing the likelihood of a single battle damage event affecting both buses.

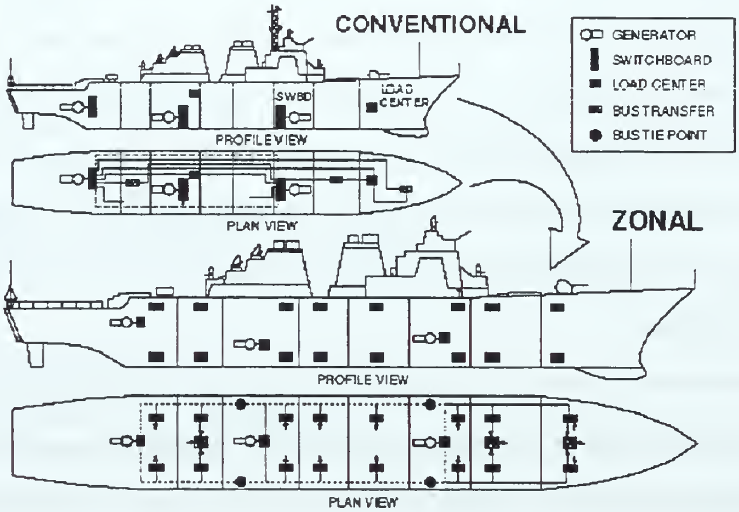


Figure I-1 Conventional Radial vs. Zonal Distribution

Therefore zonal distribution is simpler than radial. The effect of securing faulty or damaged distribution equipment is much easier to predict. Securing power to a region of the ship is straightforward. Operators trained on one ship using zonal distribution will be able to operate the zonal distribution system of another ship, even a ship of a different class, with very little training. An additional benefit from zonal distribution is that much less cabling is required, providing considerable weight and cost savings [1].

C. DC ZONAL DISTRIBUTION

If dc instead of ac transmission lines are used throughout the ship, some significant advantages may be gained. The concept of dc transmission lines used in a zonal distribution system is referred to in this thesis as DC Zonal Electrical Distribution System (DC ZEDS).

In the DC ZEDS proposed for use aboard naval surface combatants, power generated by each three-phase ac generator is rectified by a Phase-Controlled Rectifier (PCR). This dc power from each PCR is then fed to one or both main longitudinal buses. Inside each zone, power is tapped off both longitudinal buses by at least one Ship Service Converter Module (SSCM) per bus. The SSCM is a solid-state, dc-dc buck converter which steps the longitudinal bus voltage down to a lower zone voltage. This dc power at the zonal voltage level is then distributed to Ship Service Inverter Modules (SSIMs) and SSCMs within the distribution zone, each powering an ac or dc bus respectively. Individual loads which are considered vital will be powered by two or more SSIM or SSCM modules in parallel.

The DC ZEDS offers several advantages over ac zonal distribution. First, paralleling loads is straightforward when both power supplies are dc. Only the voltage must be matched. A pair of coordinated SSCMs can be easily configured to provide uninterrupted power to a load as long as one longitudinal bus has power. It is ultimately desired that a pair of converters powered from opposite main buses will supply power equally to a single vital load.

Second, variable speed ac motor control is readily achievable with DC ZEDS. Variable speed control allows for more efficient operation of large ac motors, such as those powering pumps and ventilation fans, than does constant-speed control used in the current ac distribution system.

Third, weight and space usage may both be reduced when DC ZEDS is used because the number of power conversion stages may be reduced. For example, steady dc power for some shipboard systems is supplied from 400 Hz ac. If steady dc power were readily available as it is in a DC ZEDS, then ac power would never have to be generated as an intermediate step.

A DC ZEDS shows many other advantages over ac radial distribution. In a DC ZEDS, a large number of transformers, breakers, motor controllers are replaced by fewer and smaller solid-state power converters. Generator frequency is decoupled from frequency requirements of individual ac loads. This allows optimizing generator/rectifier combinations for size and cost and facilitates operation of the prime mover at its most efficient speed.

A disadvantage of DC ZEDS is that the current state of semiconductor technology limits the bus voltage to 1500V to 2000V because of the Insulated Gate Bipolar Junction Transistors (IGBTs) and MOS Controlled Thyristors (MCTs) used in SSCMs. A very high bus voltage is desired because it will minimize current, and thus minimize the size of the conductors required. However, a higher voltage introduces safety concerns and isolation issues with the SSCMs. Future advances in semiconductor technology promise to provide higher allowable device operating voltages if required. Another small disadvantage to DC ZEDS is that shore power, supplied typically as 450 V, three-phase ac, must be rectified and converted to the dc bus voltage.

D. POWER ELECTRONIC BUILDING BLOCK

The Office of Naval Research sponsors the Power Electronic Building Block Program for design of standard modular power conversion devices. Such standardization in power electronics will reduce power system design to a task of selecting appropriate modules. A Power Electronic Building Block (PEBB) is generally a universal power processor which changes any electrical power input to any desired form of voltage, current and frequency output. A PEBB in the context of DC ZEDS is, say, an SSIM or SSCM which maintains constant output conditions regardless of the load or the number of redundant parallel modules. A PEBB module consists of a power section, a controller section, and current or voltage sensors.

E. DC ZEDS AND PEBB RESEARCH AT NPS

A number of Naval Postgraduate School theses in recent years have investigated DC ZEDS and PEBB issues. A brief overview of those efforts in order of thesis completion follows.

- A detailed SIMULINK model of a portion of a shipboard electric distribution system was developed in order to investigate control of a three-phase synchronous generator [2].
- Constant power characteristics of a DC ZEDS were investigated with reduced-order dc-dc converter models. From these PSPICE models, observations were made concerning stability and controllability [3].
- A method for using the Advanced Continuous Simulation Language (ACSL) built-in algebraic solver which neither relied upon reformulated machine representations nor introduced fictitious circuit components was developed [4].
- Work was begun on detailed ACSL modeling of dc-dc buck switching converter and a three-phase inverter. Closed-loop algorithms for buck converters were investigated, and hardware-in-the-loop studies conducted using a dSPACE card in order to validate computer models [5].
- A detailed ACSL simulation containing a steam turbine-driven synchronous machine, rectifier, filter, and buck converters was developed. This ACSL model was used to identify paralleling issues [6].
- The closed-loop buck converter algorithm was significantly advanced [7].
- A detailed ACSL representation of an Auxiliary Resonant Commutated Pole (ARCP) Inverter was developed [8].

- The one-cycle control algorithm for a buck converter was considered and implemented. Comparisons were made between the hardware and computer representation [9].
- Design and fabrication of several buck converter power sections were documented [10].
- A voltage-mode buck controller was designed, along with the required gating circuitry. The associated analog hardware was built and documented [11].
- PEBB testbed interconnecting dc-dc and dc-ac converters was fabricated. This testbed was intended to simulate various configurations of SSCM and SSIM modules. Hardware studies investigating transient response of the testbed in a few different configurations were designed and performed [12].
- The operation of the Programmable Universal Controller (PUC)—an in-house programmable DSP controller—was documented and the closed-loop algorithm for the buck controller was programmed and validated. Additionally an approach for implementing closed-loop control of ARCP inverters was suggested [13].
- Closed-loop ARCP algorithms were implemented using the PUC [14].

F. THESIS GOALS

This thesis explores design aspects of a switching controller which provides robust load sharing among an arbitrary number of dc-dc converters. This controller should support the PEBB concept by requiring no control interconnections between paralleled units. A method called frequency-based load sharing is investigated to assess its utility for DC ZEDS implementation. In addition to investigating this frequency-based load sharing control, this thesis also briefly explores the relative merits of current-mode and pulse-width-modulation (PWM) control with parallel converter operation.

G. CHAPTER OVERVIEW

Chapter II outlines pulse-width-modulation (PWM) and current-mode switch control, showing the relative benefits of each. Chapter II also includes a discussion of some strategies for the designing a switch controller for load sharing. Among the strategies compared is a new method known as frequency-based load sharing.

With that groundwork established, Chapter III explores design considerations for a simple estimation circuit which is a component of a switch controller employing frequency-based load sharing. Chapter IV documents the mathematical derivation of the models used for analysis and simulation. Finally, Chapter V discusses simulation results and Chapter VI states conclusions and recommends further related research.

II. BUCK CONVERTER

A. POWER SECTION

The bulk of this thesis deals with development of a switch controller for a dc-dc converter with good load sharing properties. The following section discusses the buck converter power section which the controller will regulate.

1. Specifications

The analysis and simulations in this thesis are performed assuming 9 kW buck converter modules. Reference output voltage (V_{ref}) is 300 V, and nominal input voltage is (V_{in}) 400V. This combination of V_{ref} and V_{in} yields a steady state duty ratio (D) of 0.75. The switching frequency (f_s) is selected to be 20 kHz, resulting in a switching period (T_s) of 50 µs. Starting with these specifications, the next section highlights critical inductance and capacitance derivations for the system used in the subsequent analysis and simulation.

2. Critical Inductance

Critical inductance, or the minimum inductance for continuous conduction mode [15], is given by

$$L_{crit} = \frac{T_s R_{LD}}{2}\left(1 - D\right) \tag{2-1}$$

where R_{LD} is the load resistance below which continuous conduction mode is maintained (100 Ω). Continuous conduction mode for loads above 10% rated is desired, thus L_{crit} is 625 µH. Since it is available in the Power Systems Laboratory, the actual inductor value assumed is 760 µH.

3. Capacitance

Experience has shown that capacitor selection is constrained by two design considerations, voltage ripple and control effort. Capacitor selection to meet the ripple criterion as developed by Fisher [15] is given by the expression

$$C = \frac{T_s\left(I_{\max} - I_{\min}\right)}{8\Delta V_c}, \tag{2-2}$$

where ΔV_C is peak-to-peak capacitor voltage ripple, and ($I_{\min} - I_{\max}$) is the inductor current envelope. The expression for ($I_{\min} - I_{\max}$),

$$I_{\max} - I_{\min} = \frac{\left(V_{in} - V_C\right)DT_s}{L} \tag{2-3}$$

also derived by Fisher [15], yields ($I_{\min} - I_{\max}$) equal to 6A. The maximum desired peak-to-peak ripple is 1%, or 3V. Thus minimum capacitance to meet the ripple criterion is 12.5 μF.

No closed-form expression exists for the second capacitor design criterion, controller effort. Simulations using pulse-width-modulation (PWM) switching control have shown that a much larger capacitor than is necessary to limit ripple voltage is required to prevent the PWM control effort from reaching its limits. A 400 μF capacitor was used successfully in PWM simulation and hardware and is used in the analyses which follow as well.

4. Load Network for Parallel Converters

Given the inductor and capacitor values derived, decisions must be made regarding how the system of parallel converters will be modeled. Specifically the type of load impedance and connection impedance between each converter's output and the node at which all outputs converge must be specified.

The load is modeled as a pure resistance in the simulations in this thesis. A resistive load is a gross simplification when, realistically, the system of parallel converters may well power an inductive load such as an inverter-driven motor, but this simplification was seen as allowable in this thesis, whose purpose is solely to explore controller design. Connecting impedances are generally modeled as a transmission line. In the context of DC ZEDS however, connecting cables within a zone will be relatively short, thus will have negligible effects from inductance. Also, the shunt capacitance will be very small and may be ignored. Thus transmission line impedance will be modeled as purely resistive. The power section for three parallel converter modules is illustrated in Figure II-1.

It should be noted that placing several buck converters in parallel, each with minimal output cable impedance, will have the same effect as placing each of the capacitors from that many converters in parallel. If the output capacitance is 400 μF for one converter, the output capacitance will be close to 1200 μF with three of those units placed in parallel. This significantly complicates the control problem because controller gains are dependent upon a constant value of the capacitance, and changing the effective capacitance by placing multiple units in parallel makes the controllers behave differently depending on how many parallel units there are. Nevertheless we want to design the converter modules with their own integral capacitors in order to support the PEBB modularity concept.

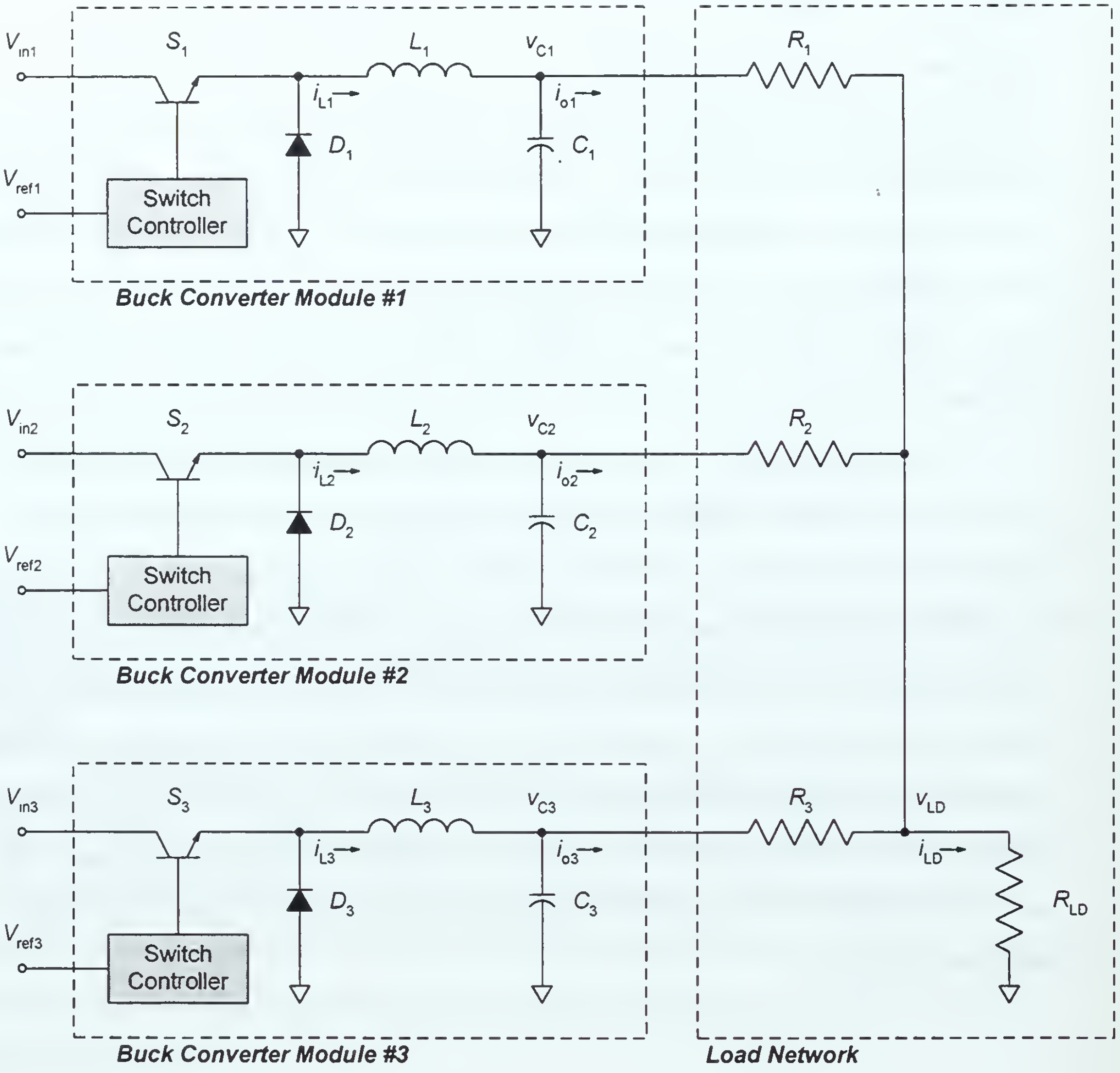


Figure II-1 Power Section Schematic

B. SWITCH CONTROLLER

The power section as described may be fitted with any of a number of types of switch controllers. PWM and current-mode control switching techniques are compared in the following pages. Both control methods considered commonly use constant switching frequency, which is also assumed in the previous L_{crit} and C derivations.

1. Pulse-Width-Modulation

The classical switch control method is pulse-width-modulation (PWM), also known as duty-ratio programming. The following discussion describes PWM by revealing the working of the switch controller blocks illustrated in Figure II-1. To that end, Figure II-2 shows the three components of the generic PWM switch controller: the PWM Control Unit, the Comparator, and the Switch Drive Unit.

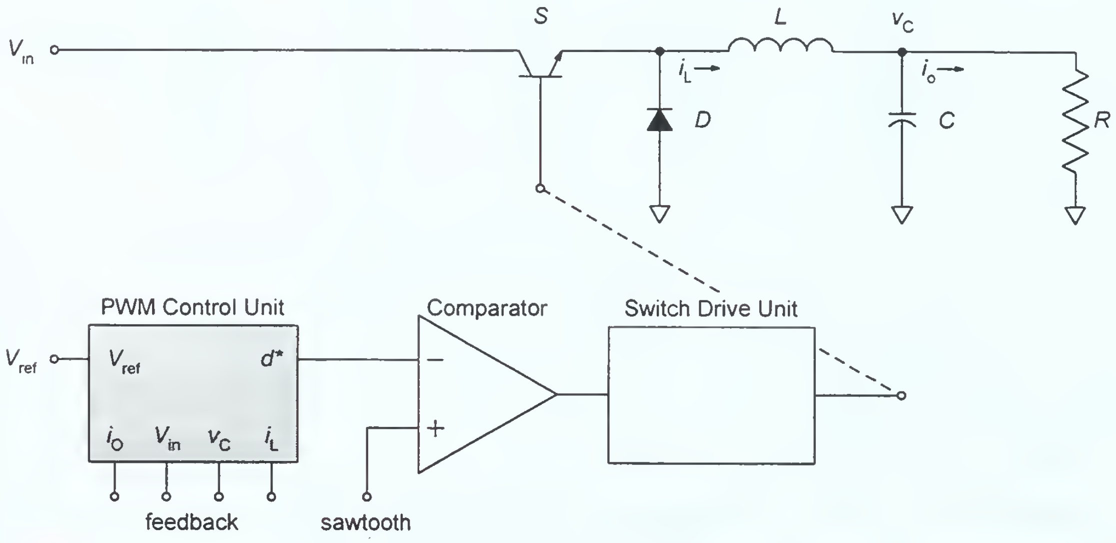


Figure II-2 PWM Switch Controller Details

a) PWM Control Unit

The PWM control unit shown uses multiloop control. That controller shown in Figure II-3 realizes the algorithm

$$d^* = \frac{V_{ref} - h_d i_o}{V_{in}} + h_v(V_{ref} - h_d i_o - v_C) + h_n \int (V_{ref} - h_d i_o - v_C)\,dt + h_i(i_L - i_o), \tag{2-4}$$

which is an expression for commanded duty ratio (d^*). This algorithm realizes PID control on capacitor voltage. The $h_i(i_L - i_o)$ term is an equivalent derivative term. [16] This algorithm also includes a droop feature. Droop is discussed later in this chapter and is represented in the above algorithm by the $(V_{ref} - h_d i_o)$ term.

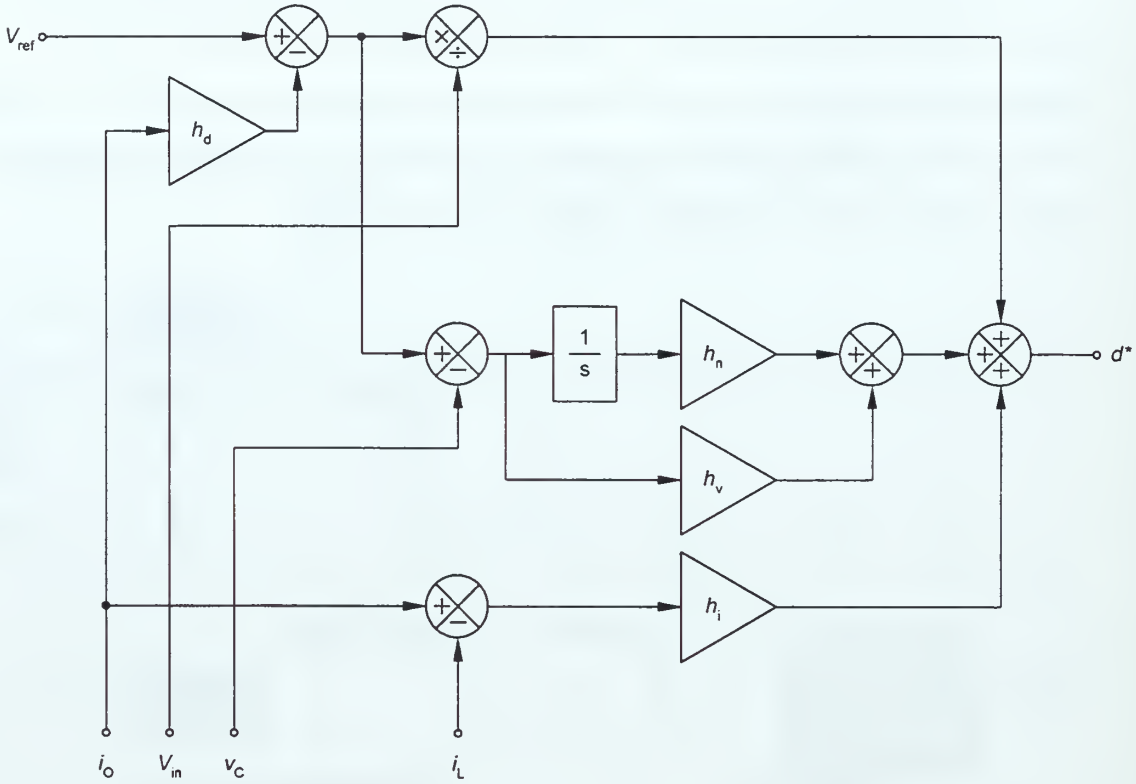


Figure II-3 PWM Control Unit

b) Comparator and Switch Drive Unit

The PWM control unit from Figure II-3 generates d^*, which is compared to a sawtooth wave. Figure II-4 illustrates the two compared signals and the comparator output. Notice that d^* is constrained to the range zero to one. Theoretically, a duty ratio equal to zero means that the switch stays off and a duty ratio equal to one means that the switch stays on. The sawtooth must stay in the range zero to one as well.

If both signals stay in the proper range, the pulse train output from the comparator will have a duty ratio equal to the commanded signal. This pulse train output from the Comparator is then fed into the Switch Drive Unit, which converts logical pulses into pulses that the particular semiconductor switch can accept. Note that the pulse train output from the controller is indicated by the shaded time slices in Figure II-4. Shaded areas are the times when the pulse is a logical zero, and non-shaded times are when the pulse is a logical one.

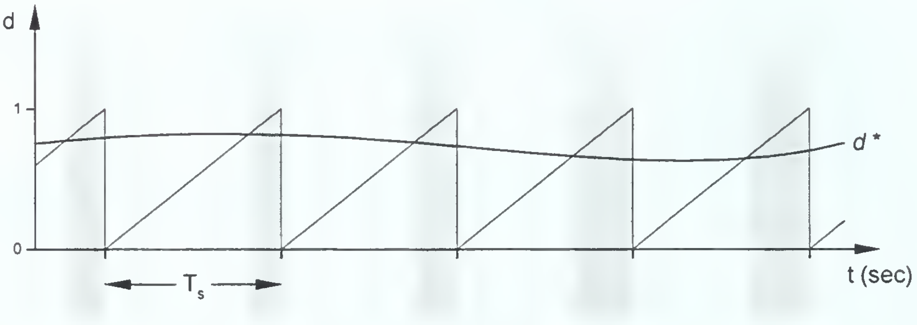


Figure II-4 PWM Switch Control

PWM is well understood and the state-space model derivation is straightforward. With PWM control, two state-space models are applicable to the system, one for when the switch is on and one when it is off. These two models may be easily collapsed to a single averaged model which removes switching dynamics but otherwise accurately describes the system as long as the inductor current remains continuous. [15]

2. Current-Mode

Current-mode switch control is now introduced and compared to PWM switch control. A block diagram of one possible current-mode implementation of the Switch Controller is shown in Figure II-5. The Switch Controller consists of five components:

the Current-Mode Control Unit, Slope Compensation, Comparator, Switch Drive Unit, and Clock.

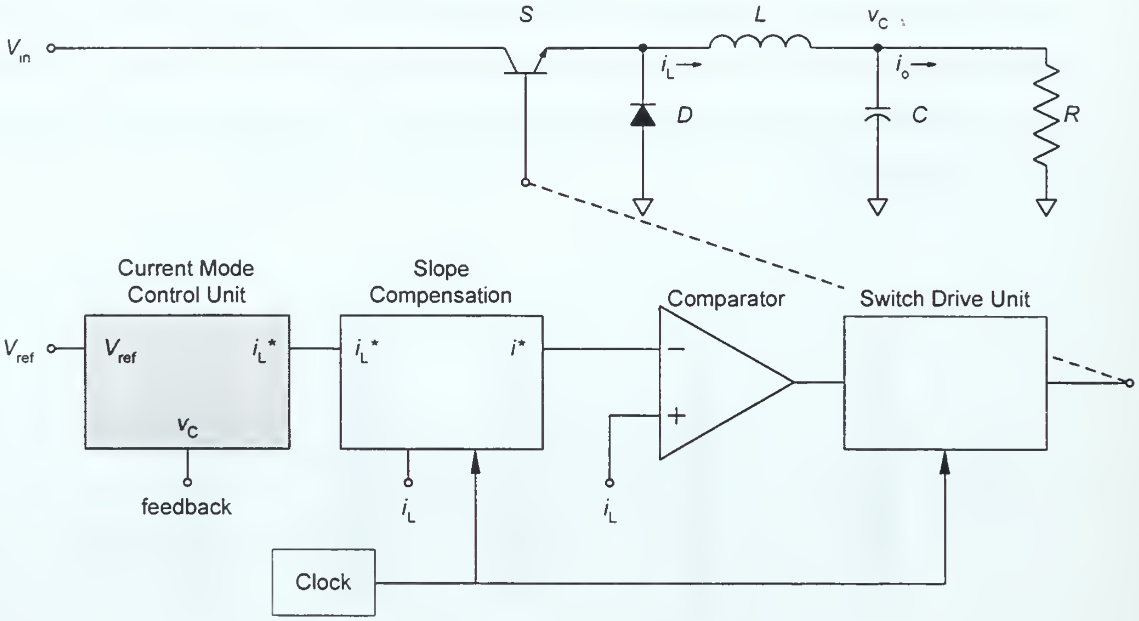


Figure II-5 Current-Mode Switch Controller Details

a) *Current-Mode Control Unit*

The Current-Mode Control Unit performs the same function as the PWM Control Unit. Namely, it generates a reference current signal using V_{ref} and various feedback signals. Figure II-6 illustrates a simple Current-Mode Control Unit. This controller realizes PI control on the voltage error, $V_{ref} - v_C$. The Current-Mode Control Unit output signal is the commanded inductor current. The algorithm realized by the controller is

$$i^* = h_n \int \left(V_{ref} - v_C\right) dt + h_v \left(V_{ref} - v_C\right). \qquad (2\text{-}5)$$

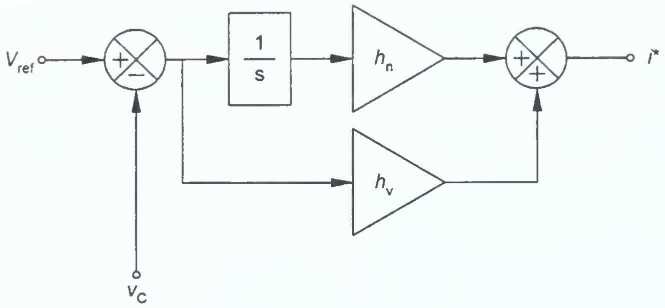


Figure II-6 Simple Current-Mode Control Unit

b) Slope Compensation

Figure II-7 shows the commanded inductor current i^* and the actual inductor current i_L for one switching period. Both i^* and i_L are comparator inputs. At the start of the switching period, i_L is increasing because the switch is closed. The switch is opened when i_L reaches i^*. At this time i_L begins to decrease as the free-wheeling diode conducts the current. Of course, i_L rises and decays exponentially due to any parasitic resistance. Since the time constant of this decay is much longer then T_s, inductor current i_L transients are represented as straight lines.

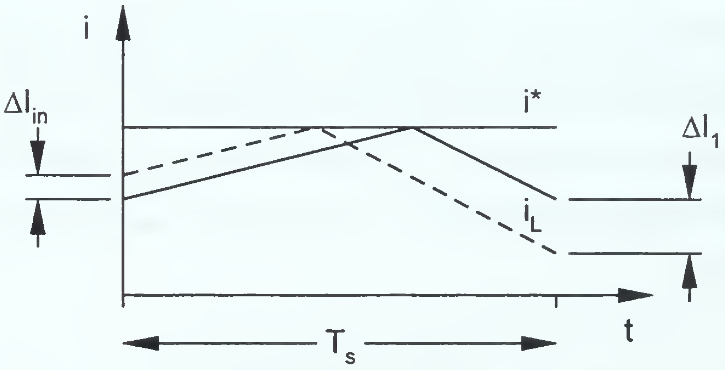


Figure II-7 Current-Mode Comparator Inputs Without Slope Compensation

Notice in Figure II-7 that when a perturbation causes i_L to be abnormally high at the start of one switching period, i_L will be low at the start of the next switching period. The dashed i_L plot in Figure II-7 shows such a perturbation. It can be shown that for one switching period, the relationship between input perturbation magnitude ΔI_{in} and output perturbation magnitude ΔI_1 is

$$\Delta I_1 = \left(\frac{-D}{1-D}\right)\Delta I_{in}, \tag{2-6}$$

where D is the steady-state duty ratio. Therefore after n switching periods, the relationship between ΔI_{in} and output perturbation magnitude ΔI_n is

$$\Delta I_n = \left(-\frac{D}{1-D}\right)^n \Delta I_{in}. \tag{2-7}$$

This equation may also be written in terms of the rising i_L slope m_1 and the falling i_L slope m_2 as follows.

$$\Delta I_n = \left(-\frac{m_2}{m_1}\right)^n \Delta I_{in}. \tag{2-8}$$

From Equation (2-7) it is apparent that for D greater than 0.5, the perturbation magnitude will grow over n switching periods.

To provide stable current-mode operation for any value of D, slope compensation is introduced. As illustrated in Figure II-8, slope compensation modifies the commanded current i^* by lowering it at a constant rate m. This modification to i^* is reset to zero at the start of each T_s. A sequence of several switching periods using slope compensation is shown in Figure II-9. The expression relating ΔI_{in} and ΔI_n with slope compensation is

$$\Delta I_n = \left(-\frac{m_2 - m}{m_1 + m}\right)^n \Delta I_{in}. \tag{2-9}$$

Therefore the rate at which i^* is modified directly affects the duty ratio below which perturbations are diminished. The ideal case is when the modifying slope m

is equal to m_2 (the rate of i_L decay with the switch open). In this case, as shown in Figure II-8, perturbations are eliminated after one switching period. [17]

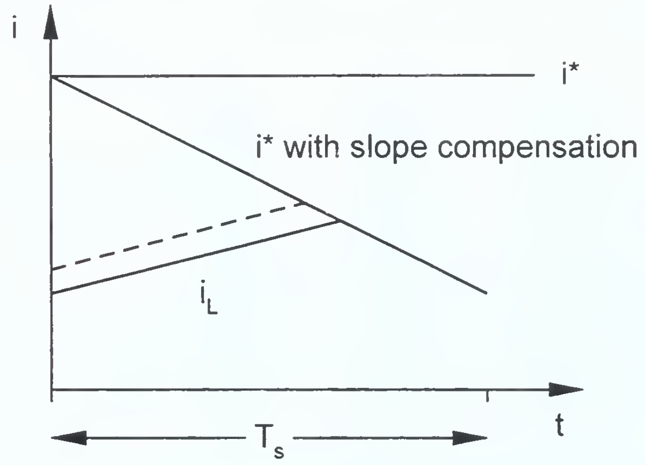


Figure II-8 Current-Mode Comparator Inputs With Slope Compensation

c) Comparator and Switch Drive Unit

Figure II-9 shows both comparator inputs for several switching periods, similar to Figure II-4 in the PWM explanation. As in Figure II-4, shaded areas in Figure II-9 indicate times when the comparator output is a logical zero, and non-shaded areas indicate times when comparator output is a logical one. Again, the switch drive unit converts logical zero and one pulses into pulses which will trigger the particular semiconductor switch.

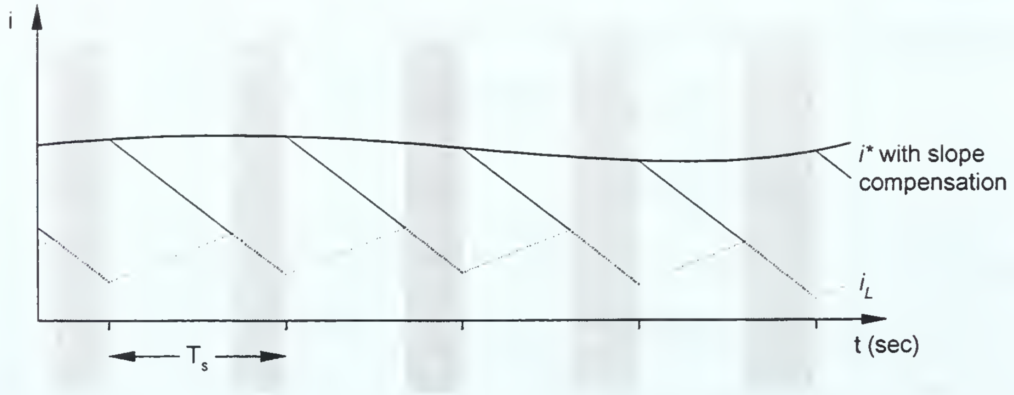


Figure II-9 Current-Mode Switch Control

d) Clock

The clock is necessary in order to turn the switch on at the beginning of every switching period. Recall that with PWM, the sawtooth drops below the commanded duty ratio signal to trigger switch turn-off. With current-mode switch control employing slope compensation, commanded and actual inductor current are equal at the end of the switching period. Therefore their comparison cannot be used to trigger switch turn-on. Instead, a clock is used to turn the switch on every switching period. The clock pulses must also be fed into the Slope Compensation circuit in order to reinitialize the slope to zero each time the switch is turned on.

C. CONTROLLER DESIGN FOR LOAD SHARING

Load sharing among converter modules is implemented by each converter in parallel forcing its output current to be close to some commanded value. Such a function is necessarily part of each converter's own switch controller. Load sharing techniques differ in that they have different sources for the commanded value of current. There are essentially two possibilities for the source of this signal—internal to the converter or from some outside source. Load sharing schemes in which converters are fed a signal from some outside source are generally known as centralized control since it is a central control unit that will generate such a signal. Load sharing schemes in which the commanded current is generated from within each power module are known as distributed control.

1. Centralized Control

With centralized control, a central unit monitors current sensed from all converters' output. The central unit then passes a commanded output signal to all converters. [18-20] Centralized control works well but has a few drawbacks. One drawback is that if an additional converter is placed in the system, the central unit must receive the new converter's sensed signals and must send that converter the commanded signal. Therefore centralized control is incompatible with the PEBB concept of having multiple converters in a system which have no control interconnections. Another drawback is that severing either the sensing lines or the command signal lines will cause the system's load sharing feature to fail while the system as a whole continues to operate. Thus system behavior is unpredictable in the event of a casualty when centralized control is used.

One version of centralized control is master-slave load sharing. With master-slave, one of the converters acts as the master, sending signals to other converters to tell them what their output currents should be [19, 21].

2. Distributed Control

Distributed control, on the other hand, is where each controller knows its share of current with no external signals applied. The traditional mechanism for distributed control is droop. With the droop method, the converter's output voltage is set based on its output current. When several converters are connected in parallel they will all have the same output voltage. Thus their currents will be forced to be equal as well. If one unit's output voltage is increased, it typically assumes a larger portion of the output current. Thus, if the reference voltage is decreased as the output current is increased, a self-regulating mechanism is put in place. Thus when voltage vs. current are plotted, the graph is the familiar "house curve." [22-23]

In previous research, droop was shown to function well when two converters are paralleled. However, load sharing performance is degraded when three or more converters are connected in parallel. Droop performance can be improved by increasing the voltage/current slope of the house curve. But if that is done, voltage will vary over a potentially unacceptable wide range.

3. Frequency-Based Load Sharing

Perreault, Selders, and Kassakian from MIT suggest a new approach to distributed control which they call frequency-based control [24]. They suggest that if each controller for a series of dc-dc converters receives an estimate of the average output current from each of the converter modules in parallel, including its own output current, then it may compare that estimate with its own output current and adjust its output to match that from the other modules. This method is new because the current estimate is a frequency-domain derived signal.

Perreault proposes three possible frequency-domain mechanisms by which converters may communicate their output current [24]. In the first method, called the output perturbation method, a small sinusoidal signal is superimposed onto the output of each converter. That signal has a frequency corresponding to the converter's own output current. Therefore at the node which connects the parallel modules, the voltage will be a dc level plus the sinusoidal components from each of the converters.

The second method, which they call isolated single-connection, uses a dedicated bus to convey current information, and not the power output cable. The third method is called switching ripple. In this method, switching frequency is adjusted corresponding to the converter's output current. In PEBB applications with a fixed switching frequency, these latter two methods are unacceptable. Thus the output perturbation method is most suitable.

Therefore when the output perturbation method is used, each converter senses its own output voltage, and from that, it analyzes the frequency content and extracts an estimate of the average frequency, then converts that to a current estimate. The perturbation generator is a simple voltage-controlled-oscillator (VCO).

The only difficulty with this new load sharing approach is in implementing an algorithm which produces an estimate of the average frequency. The method Perreault proposes is rms estimation [24].

Figure II-10 shows a block diagram of the hardware implementation of a current-mode controller employing frequency-based load sharing. The three new blocks in the diagram are the Frequency Estimator, the Perturbation Generator, and the Reference Voltage Controller. The Output Voltage Controller and Cell Power Stage are similar to the Switch Controller and Power Section as shown in Figure II-1.

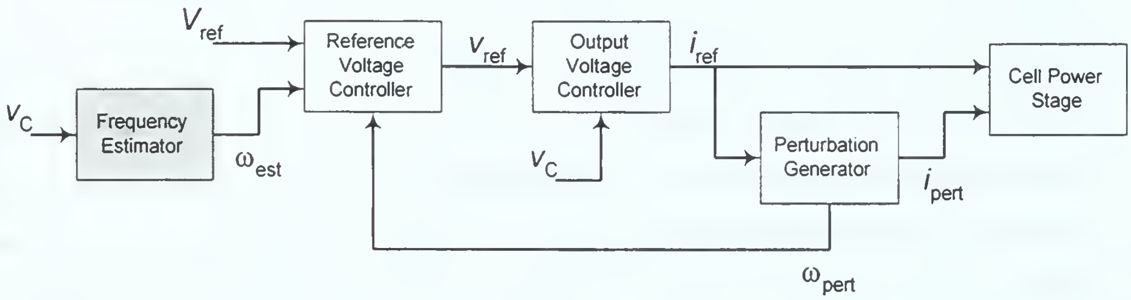


Figure II-10 Current-Mode Controller with Frequency-Based Load Sharing Block Diagram from Perreault

These three new components will be briefly discussed. The Reference Voltage Controller consists simply of a series of summing circuits which adjust V_{ref} according to the difference between ω_{pert} and ω_{est}.

The Perturbation Generator produces a sinusoid whose frequency is a function of the converter's inductor current or of commanded inductor current. The perturbation frequency range was chosen as 2 kHz to 5 kHz. This range was chosen such that perturbation frequencies fell well below the switching frequency of 20 kHz, and above the control bandwidth of approximately 1 kHz. The 2 kHz minimum perturbation frequency corresponds to zero commanded inductor current, and 5 kHz corresponds to the case where commanded current equals the converter's rated output current. Viewing the block diagram of Figure II-10, note that in addition to generating the perturbation sinusoid itself, the Perturbation Generator must also generate a signal related to the perturbation frequency. The Perturbation Generator is a relatively simple circuit, consisting of basically a VCO.

Each converter senses its own output voltage v_C for comparison with reference voltage V_{ref}. As discussed previously, voltage oscillations from parallel converters, as well as from the local converter, are present at the local converter's output. When connection resistances are small, the magnitude of the perturbations from parallel converters is attenuated very little, and the frequency content of v_C is a good approximation of the combined output. The Frequency Estimator therefore uses the oscillations on the sensed v_C signal to approximate combined output voltage perturbations from all converters and generates a signal related to the combined perturbation frequency content. Thus, each individual converter module requires no external sensors for load sharing. The Frequency Estimator is the heart of the frequency-based load sharing scheme as proposed. The next chapter explores this component in greater detail.

The block diagrams shown in this chapter have been nested. Note that in Figure II-1, a generic switch controller is shown in the shaded box. Figure II-5 shows the block diagram for that switch controller when current-mode control is used. The Current-Mode Control Unit in Figure II-5 is shown as a shaded box, and Figure II-6 shows a block diagram of that shaded box. Now, Figure II-11 shows an alternative to Figure II-6, a Current-Mode Control Unit which uses frequency-based load sharing. This block diagram in Figure II-11 is similar to that of Figure II-6. The following chapter explains the contents of the shaded Frequency Estimator block in Figure II-11.

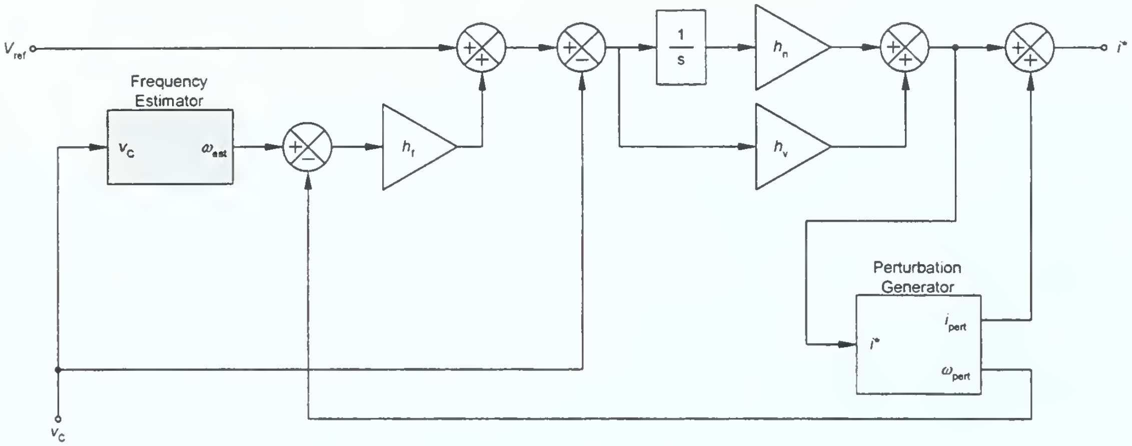


Figure II-11 Current-Mode Control Unit Employing Frequency-Based Load Sharing

III. RMS FREQUENCY ESTIMATION CIRCUIT

A. INTRODUCTION

To implement frequency-based load sharing, an estimate of the current from all converters is required. Perreault suggests rms estimation using a simple circuit [24]. Part of the research associated with this thesis involves the construction of an analog rms frequency estimation circuit similar to that described in [24]. This circuit replaces the shaded blocks in Figure II-10 and Figure II-11. The estimation circuit input is the converter module's own output voltage. Its output is a signal related to the frequency content of that output voltage. The rms estimation circuit realizes the function

$$\omega_{rms} = \frac{\sqrt{c_1^2 \omega_{pert1}^2 + c_2^2 \omega_{pert2}^2 + c_3^2 \omega_{pert3}^2}}{\sqrt{c_1^2 + c_2^2 + c_3^2}}, \tag{3-1}$$

where ω_{pert1}, ω_{pert2}, and ω_{pert3} are perturbation frequencies corresponding to the three converters' output currents; and c_1, c_2, and c_3 are weighting constants for each frequency. These constants are assumed to be unity when the perturbation signals from each converter have equal amplitude.

The proposed rms estimation circuit in [24] has four key components. A bandpass filter at the input removes frequencies from the estimation circuit input which do not contain load sharing information. That is, the switching frequency should be well above the passband and the control dynamics well below the passband. The Differentiator converts frequency to amplitude information. The RMSDC Circuit converts a sinusoidal signal into a dc level corresponding to the amplitude of oscillation. The Dividing Circuit normalizes the estimated output ω_{rms} for the input signal amplitude. A block diagram for this circuit as proposed in [24] is shown in Figure III-1.

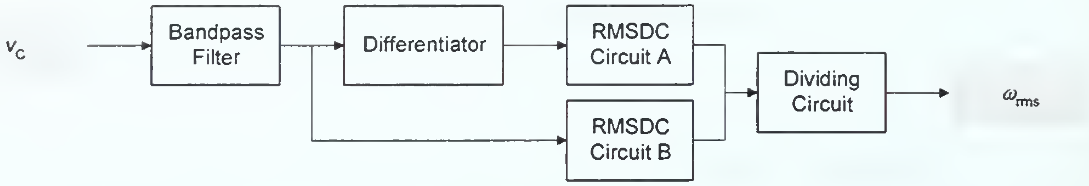


Figure III-1 Frequency Estimator Block Diagram from Perreault Paper

A schematic for the rms estimation test circuit is shown in Figure III-2. The following discussion explains the design of each sub-component.

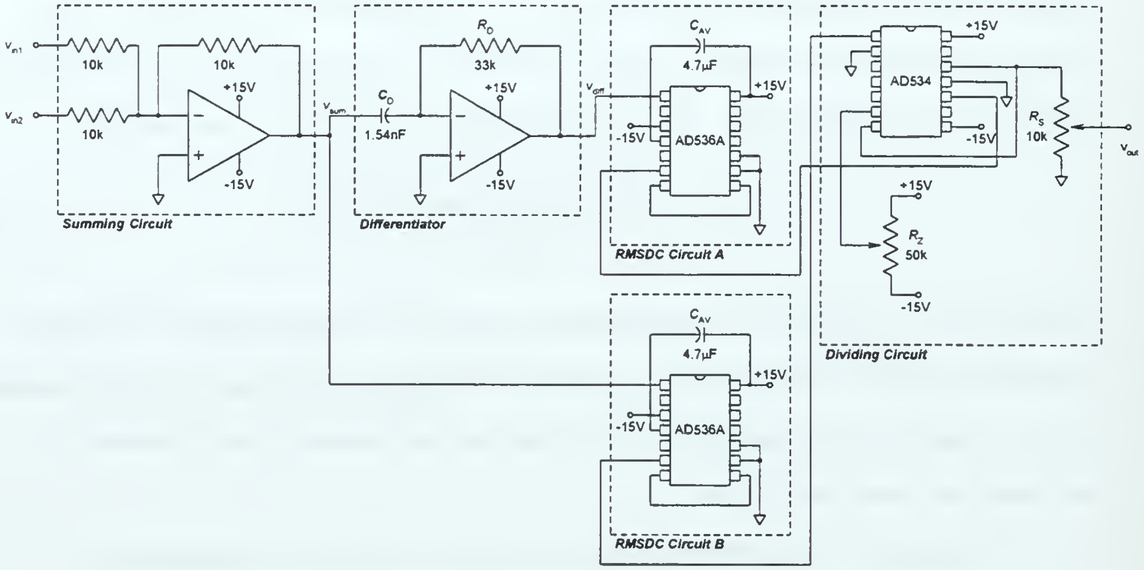


Figure III-2 RMS Frequency Estimation Test Circuit Schematic

B. TEST CIRCUIT CONSTRUCTION

1. Summing Circuit

The Summing Circuit was built in lab to simulate the output from the bandpass filter in the actual circuit. The Summing Circuit was constructed as a simple operational amplifier (op-amp) inverting summer, built as shown in Figure III-2. Input signals v_{in1} and v_{in2} were sinusoids of 0.01 V amplitude.

One notable characteristic of the Summing Circuit is that the amplitude of the output waveform has a maximum amplitude equal to twice that of the input sinusoids. Of course, this behavior is expected. One design implication is that the signal could potentially be greater than the op-amp's 15 V supply voltages when several converters are in parallel. That would cause clipping of the intermediate signal v_{sum} and inaccuracy of the estimation circuit in general.

In order to illustrate the characteristics of the Summing Circuit just discussed, a mathematical description is presented. This development shows that the output amplitude is expected to be scaled as a multiple of the number of inputs. Signals applied to v_{in1} and v_{in2} may be represented by Equations (3-2) and (3-3).

$$v_{in1} = V_1 + A_1 \sin(\omega_1 t + \theta_1) \tag{3-2}$$

$$v_{in2} = V_2 + A_2 \sin(\omega_2 t + \theta_2) \tag{3-3}$$

With the gain of each channel set to minus one, the Summing Circuit output v_{sum} (Figure III-2) is expressed as the sum of v_{in1} and v_{in2}, as shown in Equation (3-4). The inverting summer introduces minus signs into the expression.

$$v_{sum} = -v_{in1} - v_{in2} = -V_1 - V_2 - A_1 \sin(\omega_1 t + \theta_1) - A_2 \sin(\omega_2 t + \theta_2) \tag{3-4}$$

Since the Summing Circuit output simulates that of a bandpass filter, DC voltages V_1 and V_2 were fixed at zero in the lab. Thus the Summing Circuit v_{sum} output may be expressed as

$$v_{sum} = -A_1 \sin(\omega_1 t + \theta_1) - A_2 \sin(\omega_2 t + \theta_2). \tag{3-5}$$

2. Differentiator

The function of the Differentiator is key to operation of the entire rms frequency estimation circuit. The Differentiator performs a linear conversion from frequency to amplitude. An op-amp Differentiator also scales the output based on the selection of R_{D}

and C_D, the resistor and capacitor values illustrated in the Differentiator shown in Figure III-2. Thus the differentiator—and the rms estimation circuit as a whole—may be tuned so that the output is scaled appropriately for a specific range of input frequencies.

The equation governing the differentiator is

$$v_{diff} = -RC\frac{dv_{sum}}{dt}. \tag{3-6}$$

The Differentiator input is the sum of sinusoids from Equation (3-5). When v_{sum} is differentiated and multiplied by R_D and C_D, the Differentiator output is

$$v_{diff} = A_1\omega_1 R_D C_D \cos(\omega_1 t + \theta_1) + A_2\omega_2 R_D C_D \cos(\omega_2 t + \theta_2). \tag{3-7}$$

Equation (3-7) therefore shows that the peak differentiator output voltage amplitude is the sum of the input sinusoid amplitudes, A_1 and A_2, each scaled by the constant $\omega R_D C_D$. For the test circuit, R_D was chosen as 33 kΩ and C_D as 1.54 nF, thus the time constant $R_D C_D = 50.8$ μs. In the frequency range 2 kHz to 5 kHz, the angular frequency range of ω is 12,600 to 31,400 rad/sec. The corresponding range of $\omega R_D C_D$ is 0.6 (for both inputs at 2 kHz) to 1.5 (for both inputs at 5 kHz).

Obviously the choice of R_D and C_D allows flexibility in matching input and output signal levels for the Differentiator.

3. RMSDC Circuit

An AD536A performed the rms-to-dc function in both instances in the circuit. Two identical RMSDC Circuits were built and are designated *A* and *B* in Figure III-2. Both *A* and *B* circuits were set up according to the standard configuration suggested in the AD536A datasheet, which is in Appendix D, Part A. It was found that trimming neither the scale factor (pin 1) nor the offset adjust (pin 9) provided the magnitude of coarse tuning desired. For that reason, both RMSDC Circuits were constructed using the standard setup as defined in the AD536A datasheet. Scaling and offset for overall circuit output were performed at the Divider Circuit and not at each RMSDC Circuit.

Capacitor C_{AV} between pins 4 and 14 acts to damp the output response. If C_{AV} is too low—on the order of 0.1 μF—the output oscillates even when input signals have a constant frequency. If C_{AV} is to high—on the order of 40 μF—the output takes too long to reach equilibrium following a change in input. Thus the 4 μF recommended by the datasheet is a conservative value, at least for the frequencies of concern in this setup.

4. Dividing Circuit

RMSDC Circuit A, which is driven by the differentiator, has a dc output proportional to the amplitude of the input oscillations. RMSDC Circuit B has a dc output proportional to the input sinusoid amplitude and is unaffected by changes in input frequency. The Dividing Circuit realizes an $A \div B$ operation, where A and B are outputs from RMSDC Circuits A and B respectively. This function normalizes the overall circuit output, completely removing output signal dependence upon input signal amplitude. Thus, the output of the rms frequency estimation circuit is a function only of the input frequencies.

An AD534 was configured as a divider. The setup as shown in Figure III-2 is different than that recommended by the datasheet, which is in Appendix D, Part B. The datasheet configuration was not used because it produced a negative output voltage through the range of inputs expected with this circuit. The discussion that follows provides a detailed explanation of the AD534 setup as implemented in the test circuit.

The AD534 has three inputs. Each input is defined as a voltage difference between two pins. The three inputs are X ($V_{\text{pin1}} - V_{\text{pin2}}$), Y ($V_{\text{pin6}} - V_{\text{pin7}}$), and Z ($V_{\text{pin11}} - V_{\text{pin10}}$). The AD534 is governed by the equation

$$X \times Y = 10\text{V} \times Z. \tag{3-8}$$

When the AD534 output is tied to one of the Y pins, as in Figure III-2 where pins 7 and 12 are connected, then AD534 output is proportional to $Z \div X$. One of the Z pins (pin 11) and one of the X pins (pin 2) are tied to ground. The output from RMSDC

Circuit A drives Z at pin 10, and the output of RMSDC Circuit B drives X at pin 1 to such that $Z \div X$ realizes $A \div B$. Pin 6 is driven by an adjustable voltage. Adjusting V_{pin6} with potentiometer R_Z provides a zero adjust for the Dividing Circuit and for the rms frequency estimation circuit as a whole. [24]

The AD534 output driven by pin 12 is on the order of 10 V and may be too high since the estimation circuit input voltages v_{in1} and v_{in2} have amplitude on the order of 10 mV. To lower the output voltage without any loss of accuracy, a simple voltage divider scaling is used, represented by R_S (Figure III-2). Both R_Z and R_S should be chosen sufficiently large enough to limit their power consumption to within acceptable limits.

C. CIRCUIT TUNING

The rms estimation circuit was tuned to give zero output with all inputs at the nominal minimum frequency and approximately 10 mV output with all inputs at the nominal maximum frequency. Nominal minimum and maximum frequencies were chosen at 2 kHz and 5 kHz respectively. They were chosen to lie between the switching frequency of 20 kHz and the control bandwidth of approximately 1 kHz.

All output tuning is performed at the Dividing Circuit. Resistor R_Z adjusts the dc zero offset and R_S adjusts the output scaling. The procedure for tuning the circuit is as follows:

1. Set all input frequencies to nominal minimum.
2. Adjust R_Z to obtain zero volts at v_{out}.
3. Set all input frequencies to nominal maximum.
4. Adjust R_S to obtain $v_{\text{out}} = 10$ mV.

The output value of 10 mV was chosen so the output will have the same order of magnitude as the input signals. The rms estimation circuit may be designed to accommodate any reasonable input or output levels.

D. CIRCUIT PERFORMANCE

Recall that the rms frequency estimation circuit should realize Equation (3-1). After the circuit as described was constructed, tests were performed to investigate how closely the test circuit output v_{out} follows that predicted by the Equation (3-1). Static performance was analyzed to verify that the steady-state estimation circuit output was indeed a function of the input frequencies and to verify that the output was as predicted by Equation (3-1). Dynamic performance is also touched upon briefly.

1. Static Performance

To test static performance, two separate sinusoidal inputs were connected to the estimation circuit, each with an amplitude of 10 mV. One input was varied from 2 kHz to 5 kHz in 1 kHz increments while the other input was varied in the same range in 0.5 kHz increments. Input sinusoids were generated by two separate PM5134 Function Generators. Circuit output was manually recorded at each data point. Output voltage was measured using a Tektronix 2212 60 MHz Digital Storage Oscilloscope, using that instrument's digital readout.

Recall that the rms estimator test circuit was tuned for a v_{out} of zero when all input sinusoids were 2 kHz and for 10 mV when all input sinusoids were 5 kHz. Equation (3-1) does not predict frequencies in this range, however. The range of angular frequencies predicted by Equation (3-1) is 2 kHz to 5 kHz. Because of this difference, both the test circuit data and the theoretical data were normalized. After normalization, both sets of data were in the range 0 to 1, which allowed the two sets of data to be compared.

Figure III-3 shows the normalized theoretical data, predicted by Equation (3-1), and the normalized experimental data plotted together. Differences between the two sets of data are easily explained by the fact that input frequencies may not have been exactly as desired because the digital function generators were adjusted manually. With this source of error considered, the two sets of normalized data have very good correlation. It may be concluded from this static performance analysis that the rms estimation circuit proposed by [24] indeed realizes the function of Equation (3-1).

It should be noted that when the test circuit was fed two inputs of essentially equal frequency, the summing circuit produced a slowly oscillating standing wave. This standing wave had the effect of causing the estimation test circuit output to oscillate slowly. Theoretically, the same effect could occur with two nearly identical frequencies input into a bandpass filter. This standing wave should not be observed when the estimation circuit is placed in a closed-loop controller because the output from the estimation circuit will affect converter output. Thus if controller output becomes subject to this standing wave effect, converter output current will be altered, changing that converter's perturbation frequency, and finally making the two perturbation frequencies unequal, and abating the standing wave.

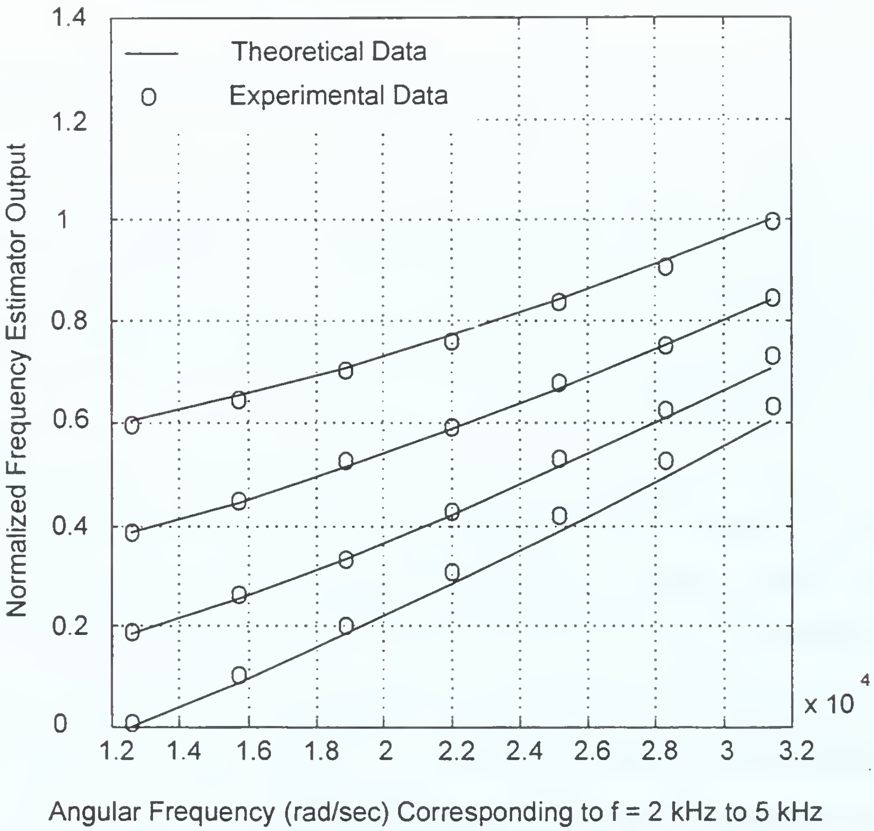


Figure III-3 Normalized Theoretical vs. Experimental Test Circuit Data

2. Dynamic Performance

No quantitative dynamic analyses were performed on the test circuit. However, some remarks may be made regarding qualitative observations of the circuit. One key observation was that the output does not reach equilibrium instantaneously upon change in the input frequency. This is because of the time constant associated with both RMSDC Circuits. Recall that capacitor C_{AV} in the RMSDC Circuits controlled the time constant. Too small a value of C_{AV} caused oscillation and too large a value of C_{AV} slowed the response unnecessarily. Therefore, C_{AV} must be chosen to satisfy both of these conflicting requirements.

E. CONSIDERATIONS FOR DESIGN AND SIMULATION

The following paragraphs summarize what was learned by evaluation of the rms-to-dc circuit and construction of the test circuit.

The output from the bandpass filter has amplitude equal to the amplitude of one input sinusoid scaled by the number of parallel converter modules. The bandpass filter should be designed such that, given the amplitude of the input frequencies in the range of interest, the output should stay well within the power supply limits (+15 V to –15 V for example) to avoid clipping.

The perturbation frequency range and amplitude should be the same for all converter modules in parallel. Even converters with different power ratings may be paralleled if the perturbation frequencies corresponding to maximum and minimum current are the same for all parallel converters.

Even though the output perturbation method is seen as the most useful implementation, the switching ripple method is a good option if variable switching frequency is allowed. With the switching ripple method, recall that switching frequency is varied according to the converter module output current. An obvious advantage with this method is that since the minimum perturbation frequency is much higher, control bandwidth may be extended as well. A disadvantage of variable switching frequency is that it produces higher switching losses. Soft switching may be required to bring switching losses down to an acceptable level, especially in converters rated at greater than 10 kW.

IV. MATHEMATICAL MODEL DEVELOPMENT

A. APPROACH TO DIGITAL SIMULATION

Previous chapters explain exactly what constitutes a current-mode converter with frequency-based load sharing. The next two chapters document the development of a mathematical representation and a digital simulation of a system of three such converter modules in parallel. The following list briefly outlines the required steps to prepare a digital simulation of the system of converters:

- Develop a state-space-averaged model for the converter power section.
- Devise a controller algorithm, with gains being unknown variables.
- Place that controller algorithm and the equations governing the power section behavior into state-space form.
- From that state-space model, derive the characteristic polynomial for the entire system with gain variables as unknowns.
- Knowing the desired system characteristic polynomial (from selected pole locations), solve the system polynomial for controller gains.
- Using those gain values, evaluate the system performance in the digital simulation.

With that framework established, it is first necessary to show the development of the controller algorithm.

B. SINGLE CONVERTER GAIN DERIVATION EXAMPLE

The following discussion outlines a simple example using the derivation steps listed above. A state-space model for a single current-mode converter is ultimately derived.

To start the derivation, it is known that two differential equations are required to represent the power section of a buck converter: One for the capacitor voltage state variable v_C and one for the inductor current state variable i_L. The differential equation governing v_C is

$$C\frac{dv_C}{dt} = i_L - i_{LD} \tag{4-1}$$

where i_L is the averaged inductor current and i_{LD} is the averaged output current. As a first approximation, the differential equation for the state variable i_L may be neglected when current-mode switching is used. Since the inductor current i_L is always very close to the commanded current i^*, the state variable may be approximated with i^*. This approximation reduces the order of the resultant state-space model and does not significantly affect system response [17]. Derivation of a system of buck converters which includes the i_L state variable is explained in Appendix A, Part A.

The starting point for a commanded current algorithm is to use the simple algorithm from Equation (2-5) which uses no load sharing mechanism. That algorithm again is

$$i^* = h_n \int (V_{ref} - v_C)dt + h_v (V_{ref} - v_C). \tag{4-2}$$

The integral term implies that the voltage error ($V_{ref} - v_C$) is a state variable. Rewriting Equation (4-2) to separate the new state variable, x, yields Equations (4-3) and (4-4).

$$i^* = h_n x + h_v (V_{ref} - v_C) \tag{4-3}$$

$$\frac{dx}{dt} = V_{ref} - v_C \tag{4-4}$$

Equations (4-1), (4-3) and (4-4) therefore describe a single current-mode-converter. Recall that when the assumption that $i_L = i^*$ is made, the expression for commanded current, Equation (4-3), is substituted into Equation (4-1). This expanded expression is

$$\frac{dv_C}{dt} = v_C\left(\frac{-1}{RC} - \frac{h_v}{C}\right) + x\left(\frac{h_n}{C}\right) + V_{ref}\left(\frac{h_v}{C}\right). \tag{4-5}$$

The two first-order differential equations from Equations (4-4) and (4-5) are now placed into state-space form, shown in Equation (4-6).

$$\frac{d}{dt}\begin{bmatrix} v_C \\ x \end{bmatrix} = \begin{bmatrix} \frac{-1}{RC} - \frac{h_v}{C} & \frac{h_n}{C} \\ -1 & 0 \end{bmatrix}\begin{bmatrix} v_C \\ x \end{bmatrix} + \begin{bmatrix} \frac{h_v}{C} \\ 1 \end{bmatrix} V_{ref} \tag{4-6}$$

The square matrix in Equation (4-6) is typically referred to as the system matrix A. Its eigenvalues, denoted by λ, are roots of the characteristic polynomial $|AI - \lambda|$. That characteristic polynomial is

$$\lambda^2 + \left(\frac{1}{RC} + \frac{h_v}{C}\right)\lambda + \left(\frac{h_n}{C}\right) = 0. \tag{4-7}$$

The coefficients of this polynomial are functions of the current-mode controller gains, h_v and h_n. The final step in determining numerical values for these gains is to solve the system for a particular desired polynomial. For example, desired system poles –1000 and –800 give the characteristic polynomial

$$\lambda^2 + 1800\lambda + 800{,}000 = 0. \tag{4-8}$$

To calculate gains h_v and h_n which provide system response identical to the system with the characteristic polynomial given by Equation (4-8), the coefficients of like powers of λ in Equations (4-7) and (4-8) must be equal. Thus the following two expressions apply.

$$1800 = \left(\frac{1}{RC} + \frac{h_v}{C}\right) \tag{4-9}$$

$$800{,}000 = \frac{h_n}{C} \tag{4-10}$$

Capacitance C, as stated earlier, is 400 μF. Load resistance R at full load is 10 Ω. The gains are found to be $h_v = 0.62$ and $h_n = 320$. The Matlab m-file with which these gains were computed is shown in Appendix B, Part A. That single-converter model may be used to calculate gains when desired poles are given or to calculate system poles when gains are given.

C. CONTROLLER ALGORITHM DERIVATION

The preceding example illustrates the basic process by which controller gains are calculated. Complexity will now be added to the model discussed previously, and the same steps taken to derive controller gains.

At the outset of this research, it was desired to incorporate frequency-based load sharing, as introduced by [24], into a PWM switch control scheme. All converters constructed to date in the DC ZEDS use PWM switch control. Adding the frequency-based circuitry to the existing controller framework was the first logical step. The controller algorithm therefore would be similar to that of Equation (2-4). That commanded duty ratio algorithm for a PWM controller, employing droop load sharing, is repeated in Equation (4-11) for convenience.

$$d^* = \frac{V_{ref} - h_d i_o}{V_{in}} + h_v (V_{ref} - h_d i_o - v_C) + h_n \int (V_{ref} - h_d i_o - v_C) dt + h_i (i_o - i_L) \quad \text{(4-11)}$$

Droop load sharing will be replaced with frequency-based load sharing. When the droop-related terms are removed from this algorithm as a step toward adding frequency-based load sharing, the equation becomes

$$d^* = \frac{V_{ref}}{V_{in}} + h_v (V_{ref} - v_C) + h_n \int (V_{ref} - v_C) dt + h_i (i_o - i_L). \quad \text{(4-12)}$$

Adding frequency-based load sharing requires modifying V_{ref} in proportion to the frequency error $(\omega_{est} - \omega_{pert})$. Since the perturbation frequency is a linear function of commanded inductor current, this frequency error represents current error. Incorporating such a term into the algorithm of Equation (4-12) gives

$$d^* = \frac{V_{ref} - h_f(\omega_{est} - \omega_{pert})}{V_{in}} + h_v(V_{ref} - h_f(\omega_{est} - \omega_{pert}) - v_C) + h_n \int \left(V_{ref} - h_f(\omega_{est} - \omega_{pert}) - v_C\right)dt + h_i\left(i_o - i_L\right) \tag{4-13}$$

where load sharing gain h_f is yet to be determined.

A digital simulation was developed for two converters using Equation (4-13). That simulation showed that system performance with unequal connection resistances was unsatisfactory. Each converter's output current tended to oscillate about the desired value before settling after a transient. It was speculated that this oscillatory behavior was caused by the fact that PWM does not control current directly. Because of these unsatisfactory simulation results, the research effort was redirected toward an investigation of current-mode control. In addition, current-mode control was employed in Perreault's work.

Perreault [24] does not recommend any particular controller algorithm. A suitable control algorithm was needed. It was decided to use as simple an algorithm as possible and add complexity as needed to correct problems. The starting point for choosing an algorithm is the control law introduced in Equation (2-5). That algorithm is as follows.

$$i^* = h_n \int \left(V_{ref} - v_C\right)dt + h_v\left(V_{ref} - v_C\right) \tag{4-14}$$

This algorithm implements proportional-integral (PI) control on the voltage error. Integral control maintains zero steady-state voltage error. Proportional control provides transient stability. Adding frequency-based load sharing to this algorithm is accomplished much the same way as for PWM in Equation (4-13). Reference voltage V_{ref} is modified in proportion to the frequency error. The resulting algorithm is

$$i^* = h_n \int \left(V_{ref} - h_f\left(\omega_{est} - \omega_{pert}\right) - v_C\right)dt + h_v\left(V_{ref} - h_f\left(\omega_{est} - \omega_{pert}\right) - v_C\right). \tag{4-15}$$

D. TWO-CONVERTER STATE-SPACE DERIVATION

With this control algorithm decided upon, the next step is to put the entire two-converter system into state-space form. A system of two or more parallel converters must be represented in a single state-space model because the output voltage of each depends on the output current of all converters.

Equation (4-1) governs the power section behavior, as in the single-converter model. The inductor current state variable i_L is neglected, as in the single-converter derivation. The only change is that two converters are modeled together, and that the switching control algorithm for both is as defined in Equation (4-15). Subscripts are added to the terms in the following derivations to distinguish between converter 1 and 2.

Consider a two-converter system similar to the three-converter system of Figure II-1. Rewriting Equations (4-1) and (4-15) to include subscripts and to include the connection resistances network, the following two expressions are derived.

$$C_1 \frac{dv_{C1}}{dt} = i_{L1} - i_{o1} \tag{4-16}$$

$$i_1{*} = h_{n1} \int \left(V_{ref1} - h_{f1}\left(\omega_{est} - \omega_{pert1}\right) - v_{C1}\right) dt + h_{v1}\left(V_{ref1} - h_{f1}\left(\omega_{est} - \omega_{pert1}\right) - v_{C1}\right) \tag{4-17}$$

Equation (4-17) is rewritten as two equations to separate state variable x_1, as shown in Equations (4-18) and (4-19).

$$i_1{*} = h_{n1} x_1 + h_{v1}\left(V_{ref1} - h_{f1}\left(\omega_{est} - \omega_{pert1}\right) - v_{C1}\right) \tag{4-18}$$

$$\frac{dx_1}{dt} = V_{ref1} - h_{f1}\left(\omega_{est} - \omega_{pert1}\right) - v_{C1} \tag{4-19}$$

Again making the assumption that $i_1{*} = i_{L1}$, i_{L1} in Equation (4-16) is replaced by the expression for $i_1{*}$ of Equation (4-18). Equation (4-16) rewritten after that substitution is

$$\frac{dv_{C1}}{dt} = \frac{h_{n1} x_1}{C_1} + \frac{h_{v1}}{C_1}\left(V_{ref1} - h_{f1}\left(\omega_{est} - \omega_{pert1}\right) - v_{C1}\right) - \frac{i_{o1}}{C_1}. \tag{4-20}$$

Expressions for converter 2, similar to those in Equations (4-19) and (4-20) for converter 1, are

$$\frac{dx_2}{dt} = V_{ref2} - h_{f2}\left(\omega_{est} - \omega_{per2}\right) - v_{C2} \tag{4-21}$$

$$\frac{dv_{C2}}{dt}=\frac{h_{n2}x_2}{C_2}+\frac{h_{v2}}{C_2}\left(V_{ref2}-h_{f2}\left(\omega_{est}-\omega_{pert2}\right)-v_{C2}\right)-\frac{i_{o2}}{C_2}. \tag{4-22}$$

Considering only converter 1 in the derivation, note that Equations (4-19) and (4-20) cannot be placed into state-space form because neither is expressed entirely in terms of state variables. Converter module output current i_{o1} and the frequency error (ω_{est} – ω_{pert1}) must be expressed in terms of state variables v_{C1}, x_1, v_{C2}, and x_2. Derivation of these quantities is presented in Appendix A, Parts B and C. The resulting expressions are as follows.

$$i_{o1}=v_{C1}\left(\frac{R_2+R_{LD}}{\alpha_2}\right)+v_{C2}\left(\frac{-R_{LD}}{\alpha_2}\right) \tag{4-23}$$

$$i_{o2}=v_{C1}\left(\frac{-R_{LD}}{\alpha_2}\right)+v_{C2}\left(\frac{R_1+R_{LD}}{\alpha_2}\right) \tag{4-24}$$

$$\left(\omega_{avg}-\omega_{pert1}\right)=\frac{\beta}{2\alpha_2}\left[v_{C1}\left(-R_2-2R_{LD}\right)+v_{C2}\left(R_1+2R_{LD}\right)\right] \tag{4-25}$$

$$\left(\omega_{avg}-\omega_{pert2}\right)=\frac{\beta}{2\alpha_2}\left[v_{C1}\left(R_2+2R_{LD}\right)+v_{C2}\left(-R_1-2R_{LD}\right)\right] \tag{4-26}$$

where α_2 and β are defined in the aforementioned Appendix subsections.

Considering still converter 1, Equations (4-20), (4-23), and (4-25) are combined into a single expression as follows.

$$\frac{dv_{C1}}{dt}=v_{C1}\left(a_{11}\right)+x_1\left(a_{12}\right)+v_{C2}\left(a_{13}\right)+V_{ref}\left(b_{11}\right) \tag{4-27}$$

where

$$a_{11}=\frac{-h_{f1}h_{v1}\beta}{2C_1\alpha_2}\left(-R_2-2R_{LD}\right)-\frac{h_{v1}}{C_1}-\frac{R_2+R_{LD}}{C_1\alpha_2} \tag{4-28}$$

$$a_{12}=\frac{h_{n1}}{C_1} \tag{4-29}$$

$$a_{13}=\frac{-h_{f1}h_{v1}\beta}{2C_1\alpha_2}\left(R_1+2R_{LD}\right)+\frac{R_{LD}}{C_1\alpha_2} \tag{4-30}$$

$$b_{11} = \frac{h_{v1}}{C_1}. \tag{4-31}$$

Equations (4-19) and (4-25) for converter 1 are combined into the single equation

$$\frac{dx_1}{dt} = v_{C1}\left(-1 + \frac{h_{f1}\beta}{2\alpha_2}\left(R_2 + 2R_{LD}\right)\right) + v_{C2}\left(\frac{-h_{f1}\beta}{2\alpha_2}\left(R_1 + 2R_{LD}\right)\right) + V_{ref1}. \tag{4-32}$$

This equation it rewritten for clarity as

$$\frac{dx_1}{dt} = v_{C1}\left(a_{21}\right) + v_{C2}\left(a_{23}\right) + V_{ref1} \tag{4-33}$$

where

$$a_{21} = -1 + \frac{h_{f1}\beta}{2\alpha_2}\left(R_2 + 2R_{LD}\right) \tag{4-34}$$

and

$$a_{23} = \frac{-h_{f1}\beta}{2\alpha_2}\left(R_1 + 2R_{LD}\right). \tag{4-35}$$

Equations (4-27) and (4-33) constitute the state-space representation for converter 1. A similar state-space representation is derived for converter 2 and is given by Equations (4-36) and (4-41). The expression for the converter 2 output voltage state variable is

$$\frac{dv_{C2}}{dt} = v_{C1}\left(a_{31}\right) + v_{C2}\left(a_{33}\right) + x_2\left(a_{34}\right) + V_{ref2}\left(b_{32}\right) \tag{4-36}$$

where

$$a_{31} = \frac{-h_{f2}h_{v2}\beta}{2C_2\alpha_2}\left(R_2 + 2R_{LD}\right) + \frac{R_{LD}}{C_2\alpha_2} \tag{4-37}$$

$$a_{33} = \frac{-h_{f2}h_{v2}\beta}{2C_2\alpha_2}\left(-R_1 - 2R_{LD}\right) - \frac{h_{v2}}{C_2} - \frac{R_1 + R_{LD}}{C_2\alpha_2} \tag{4-38}$$

$$a_{34} = \frac{h_{n2}}{C_2} \tag{4-39}$$

$$b_{32} = \frac{h_{v2}}{C_2}. \tag{4-40}$$

The expression for the converter 2 controller integral state variable is

$$\frac{dx_2}{dt} = v_{C1}\left(a_{41}\right) + v_{C2}\left(a_{43}\right) + V_{ref2} \tag{4-41}$$

where

$$a_{41} = \frac{-h_{f2}\beta}{2\alpha_2}\left(R_2 + 2R_{LD}\right). \tag{4-42}$$

and

$$a_{43} = -1 + \frac{h_{f2}\beta}{2\alpha_2}\left(R_1 + 2R_{LD}\right). \tag{4-43}$$

The entire system of two buck converters with current-mode switch control and frequency-based load sharing is written as

$$\frac{d}{dt}\begin{bmatrix} v_{C1} \\ x_1 \\ v_{C2} \\ x_2 \end{bmatrix} = \begin{bmatrix} a_{11} & a_{12} & a_{13} & 0 \\ a_{21} & 0 & a_{23} & 0 \\ a_{31} & 0 & a_{33} & a_{34} \\ a_{41} & 0 & a_{43} & 0 \end{bmatrix}\begin{bmatrix} v_{C1} \\ x_1 \\ v_{C2} \\ x_2 \end{bmatrix} + \begin{bmatrix} b_{11} & 0 \\ 1 & 0 \\ 0 & b_{32} \\ 0 & 1 \end{bmatrix}\begin{bmatrix} V_{ref1} \\ V_{ref2} \end{bmatrix} \tag{4-44}$$

where a_{xx} and b_{xx} are defined in Equations (4-28) to (4-31), (4-34) to (4-35), (4-37) to (4-40), and (4-42) to (4-43) above. This state-space model was coded in a Matlab file, which is shown in Appendix B, Part C.

E. DERIVATION SIMPLIFICATION

At this point, it is constructive to consider the remainder of the derivation. A state-space model is now available, as shown in Equation (4-44). Recall from Part A of this chapter that the next step in the derivation is to express the system matrix characteristic polynomial in terms of the unknown gains. Several difficulties are encountered in taking this next step.

The first difficulty lies in the fact that more unknown gains exist than polynomial degrees. With three unknown gains h_n , h_v , and h_f from each converter, there are a total of six gains in the two-converter system. The gains cannot be found explicitly. The simplifying assumption which makes the most sense is that the integral gains for each controller are equal ($h_{n1} = h_{n2}$), as well as proportional gains ($h_{v1} = h_{v2}$). With this assumption, the number of unknown gains is four, and may be found by solving the fourth-order polynomial.

A more worrisome observation is that finding a closed-form expression for gains, given Equation (4-44) as a starting point, is very difficult. Obtaining a polynomial from the state-space model, as shown in the step between Equations (4-6) and (4-7), requires finding an expression for eigenvalues λ of the system matrix $\boldsymbol{A}$ by calculating $|\lambda I - \boldsymbol{A}|$. The 4×4 system shown in Equation (4-44) is rather complex and yields an unwieldy result.

To overcome this difficulty, another simplifying assumption is made. Since the connection resistances are small relative to the load resistance, the effect of paralleling modules may be approximated simply by paralleling the output capacitors. Thus, multiple buck modules may be replaced by a single buck with appropriately increased output capacitance. Controller gains are therefore approximated by using the single-converter model with no load sharing and changing the value of C according to the number of parallel modules.

The single-converter characteristic polynomial in Equation (4-7) is altered by replacing C with $(2 \times C)$, thus representing the additional capacitance added by a second converter in parallel. Load resistance R in Equation (4-7) must be changed as well because the rated power for two converters in parallel is twice that of a single converter. Minimum load resistance for the two-converter case is half that of the single-converter case. The table below shows load resistance and filter capacitance appropriate for estimating one-, two- or three-converter systems at full load or 10% rated load.

	Load (%)	R (Ω)	C (μF)	h_n	h_v
One Converter:	100	10	400	0.62	320
One Converter:	10	100	400	0.71	320
Two Converters:	100	5	800	1.24	640
Two Converters:	10	50	800	1.42	640
Three Converters:	100	3.33	1200	1.86	960
Three Converters:	10	33.3	1200	2.13	960

Table IV-1 Simplified Gain Derivations

Thus gains are approximated. Recall that the single-converter system used for calculating this approximation used no load sharing mechanism. No values for load sharing gain h_f are calculated in this approximation. Load sharing gains will be found by trial and error once the simulation is run.

It is desired to see how well this approximation for the two-converter system gain calculation works. To evaluate, appropriate gains are placed into the detailed Matlab representation for the two-converter system. Those gains used are $h_n = 1.24$ and $h_v = 640$. Load sharing gains h_f are set to zero for comparison purposes. Recall from Part B of this chapter that the desired system poles are –800 and –1000. The expected poles for the two-converter system if this approximation were perfectly accurate, are two at –800 and two at –1000. The Matlab m-file in Appendix B, Part C is set up to calculate system poles when the above values of gains h_n and h_v are used for both converter module controllers. Connection resistances R_1 and R_2 are 1 mΩ. The resulting poles from this test are: –2.5031e+6, –2612.6, –612.42, and –0.63921.

The poles for the system with approximated gains are all real, just as the desired poles for the single-converter system are. Notice however that the lowest pole is –0.6 compared with –800, and the largest pole is –2e+6 as opposed to –1e–3. Therefore the simulation for the two-converter system using these approximated gains will not have the same transient response as a single converter. It is hoped that these gains are close enough to provide a stable simulation with which load sharing properties among two converters can be tested.

F. POLE SELECTION

It was asserted in Part B of this chapter that the desired system poles are real poles of –800 and –1000 and no explanation was given. These poles were found to give good system response when used in the single-converter current-mode system with no load sharing mechanism. Gains h_v and h_n were adjusted to minimize voltage overshoot and settling time for a load step change transient. The gains which were found by trial and error provided voltage spikes of less than 5 V when the step load change was 100% to 20%. The poles associated with these gains are different from those first attempted. First, a slightly underdamped two-pole system was used. It was found that simulation with those system poles showed too oscillatory a response. Future work should include a method of finding desired system poles.

V. SIMULATION

A. ADVANCED CONTINUOUS SIMULATION LANGUAGE MODEL

The previous chapter presented derivations that were the basis for the determination of gains. The end goal of that exercise is to obtain gains for use in the digital simulation such that the system will have a suitable transient performance. Construction of the simulation model itself is relatively straightforward. All that is required is to represent the system governing equations in the syntax of the simulation language. The simulation tool used for this thesis is the Advanced Continuous Simulation Language (ACSL). The simulation was constructed in ACSL for a system of three parallel current-mode-switched buck converters using frequency-based load sharing.

As derived in Chapter IV, the set of equations which fully describe a buck converter using current-mode switch control and frequency-based load sharing are the following. Subscripts indicate that these equations are for converter module number 1.

$$\frac{dv_{C1}}{dt} = \frac{h_{n1}x_1}{C_1} + \frac{h_{v1}}{C_1}\left(V_{ref1} - h_{f1}\left(\omega_{est} - \omega_{pert1}\right) - v_{C1}\right) - \frac{i_{o1}}{C_1} \tag{5-1}$$

$$\frac{dx_1}{dt} = V_{ref1} - h_{f1}\left(\omega_{est} - \omega_{pert1}\right) - v_{C1} \tag{5-2}$$

$$i_{o1} = v_{C1}\left(\frac{R_2 + R_{LD}}{\alpha_2}\right) + v_{C2}\left(\frac{-R_{LD}}{\alpha_2}\right) \tag{5-3}$$

$$\left(\omega_{avg} - \omega_{pert1}\right) = \frac{\beta}{2\alpha_2}\left[v_{C1}\left(-R_2 - 2R_{LD}\right) + v_{C2}\left(R_1 + 2R_{LD}\right)\right] \tag{5-4}$$

Constants α_2 and β are defined in Appendix A, Parts B and C.

An ACSL representation for a system of three converters was constructed and is shown in Appendix C. Both the .csl file and the .cmd file are listed. The body of the .csl file was obtained from previous research work. That original .csl file was a detailed simulation for a single PWM-switched buck converter, which allowed for both continuous and discontinuous conduction modes. Modifications to the switching rules were made to this file in order to simulate current-mode switching. The algorithm for the commanded current, as shown by Equations (5-1) to (5-4) above, replaced that for commanded duty ratio in the original file. Multiple converter modules are realized in the simulation by duplicating the governing equations for power section and controller section. Numerical subscripts are added to distinguish between the three converters represented. The dynamics of the resistance network in the power section required the use of the load voltage v_{LD} and load current i_{LD} derivations in terms of state variables for three converters, as described in Appendix A, Parts 1 b) and 2 b).

As stated in Chapter IV, the gains for a multi-converter system are approximated by assuming a large aggregate converter and are not calculated explicitly. The approximated gains for one-, two-, and three-converter configurations at 100% and 10% load are summarized in Table IV-1. Referencing this table, $h_v = 960$ and $h_n = 1.96$ are appropriate for three parallel converters operating over a range of loading conditions.

Load sharing gains h_{f1}, h_{f2}, h_{f3} are chosen experimentally. These gains are chosen at 0.01 because the load sharing performance has been proven with these values, and the system performance for which PI gains are chosen to optimize was not terribly compromised.

B. LOAD SHARING PERFORMANCE

1. Connection Resistance Effects

A robust load-sharing mechanism will allow approximately equal current from all parallel converters when connection resistances are unequal. One ACSL simulation was run with connection resistances R_1, R_2, and R_3 equal to 0.02, 0.04, and 0.05 Ω respectively. All frequency-based load sharing gains h_{f1}, h_{f2}, h_{f3} were set at 0.01. Figure V-1 shows the output from that simulation.

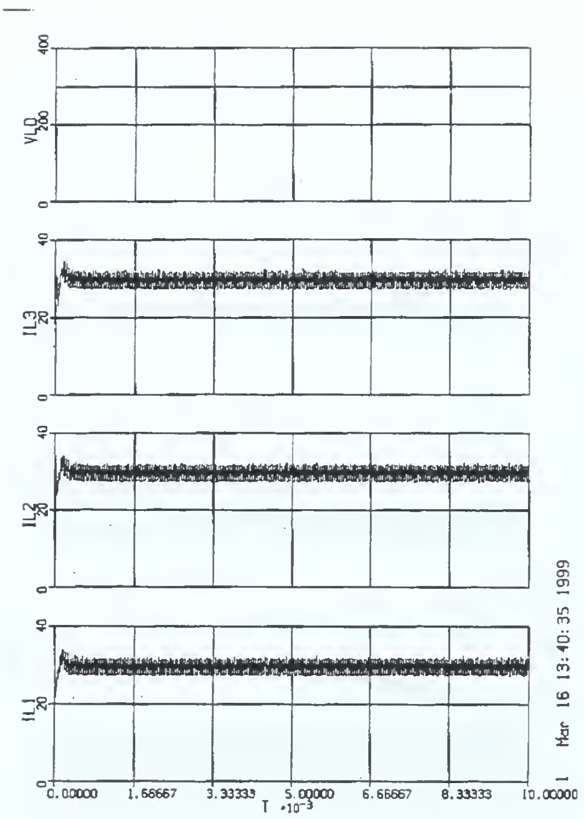


Figure V-1 ACSL Simulation: Different Connection Resistances, Load Sharing Employed

As is evident in Figure V-1, inductor current stabilizes quickly to a value very close to that of the other modules.

Figure V-2 shows the same simulation as in Figure V-1 except with load sharing gains h_{f1}, h_{f2}, h_{f3} set to zero. This simulated system fails to adequately share current and illustrates the need for a load sharing mechanism.

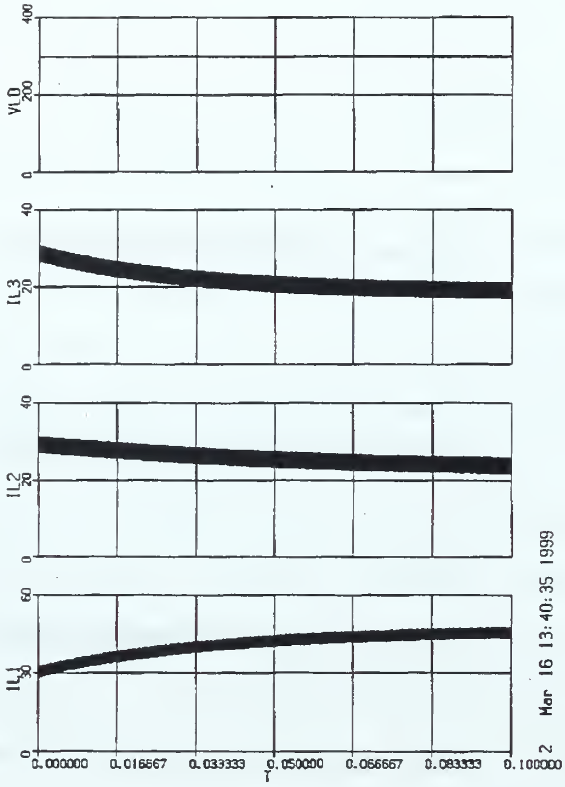


Figure V-2 ACSL Simulation: Different Connection Resistances, No Load Sharing

2. Reference Voltages Effects

A rigorous test of the frequency-based load sharing scheme was considered as the case where reference voltages were unequal. Figure V-3 shows simulation output for the unequal reference voltages where $V_{ref1} = 280$ V, $V_{ref2} = 300$ V, and $V_{ref3} = 320$ V. In Figure V-3 also, load sharing was used and h_{f1}, h_{f2}, h_{f3} are set to 0.01.

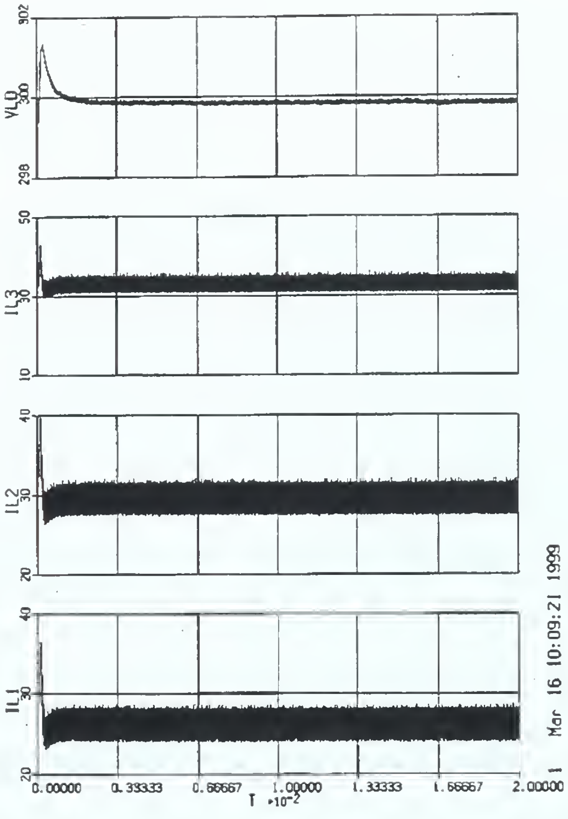


Figure V-3 ACSL Simulation: Three Converters, Unequal Reference Voltages, Load Sharing Employed

That same simulation was run without load sharing, with h_{f1}, h_{f2}, h_{f3} set to 0.0. Results of that simulation are shown in Figure V-4. The other parameters are unchanged from the simulation of Figure V-3. It is apparent that unequal reference voltages cause load sharing to fail. Figure V-3 shows that with load sharing, inductor currents are still not equal. The system may be designed for better performance by increasing h_f if it is suspected that unequal reference voltages of this magnitude are possible. In general, however, such large discrepancies between reference voltages is not expected.

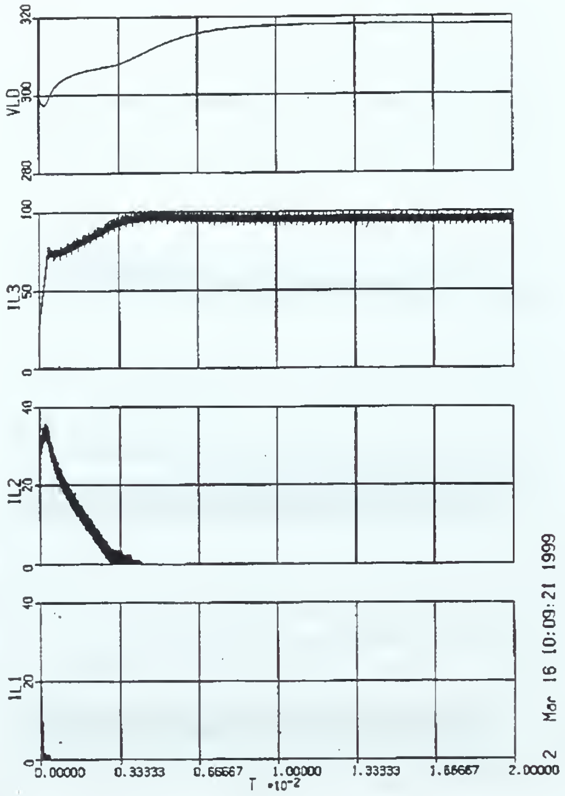


Figure V-4 ACSL Simulation: Three Converters, Unequal Reference Voltages, No Load Sharing

C. TRANSIENT PERFORMANCE

The preceding discussion showed that the load sharing characteristics of the group of parallel converters works well when frequency-based load sharing is employed. Transient stability must also be considered. Recall that the controller gains were not selected to provide precise system poles but were instead approximated. The system is expected to perform marginally when gains are selected in this manner. The two simulation results show that this is indeed the case.

Figure V-5 shows simulation output for a step load change from 100% to 20%. Both the voltage spike of 20 V and the tendency of current to increase before settling at a lower steady-state value are undesirable.

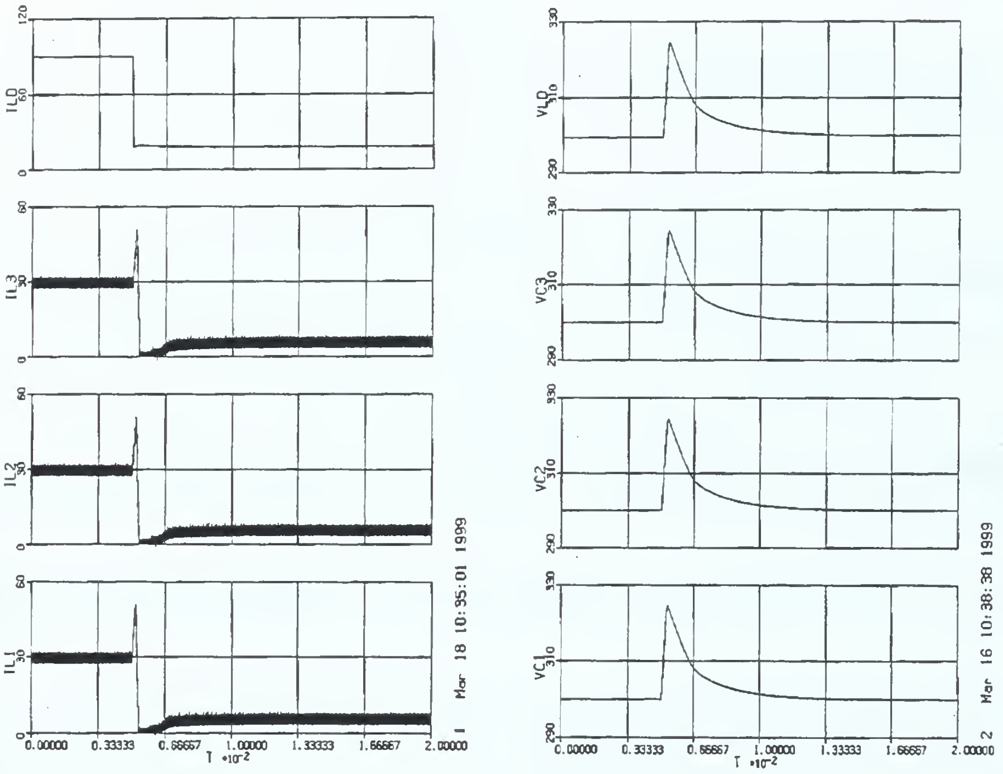


Figure V-5 ACSL Simulation: Three Converters, Step Load Change From 100% to 20%

Figure V-6 shows simulation results for the case of three converters online with one abruptly shut down. A converter would be brought on or off line by slowly ramping reference voltage up or down. The simulation of Figure V-6 is intended to prove performance in worst-case conditions, where one redundant power supply is perhaps lost due to battle damage. As with the step load change simulation, transient performance is marginal. This situation will hopefully be remedied by more careful gain selection.

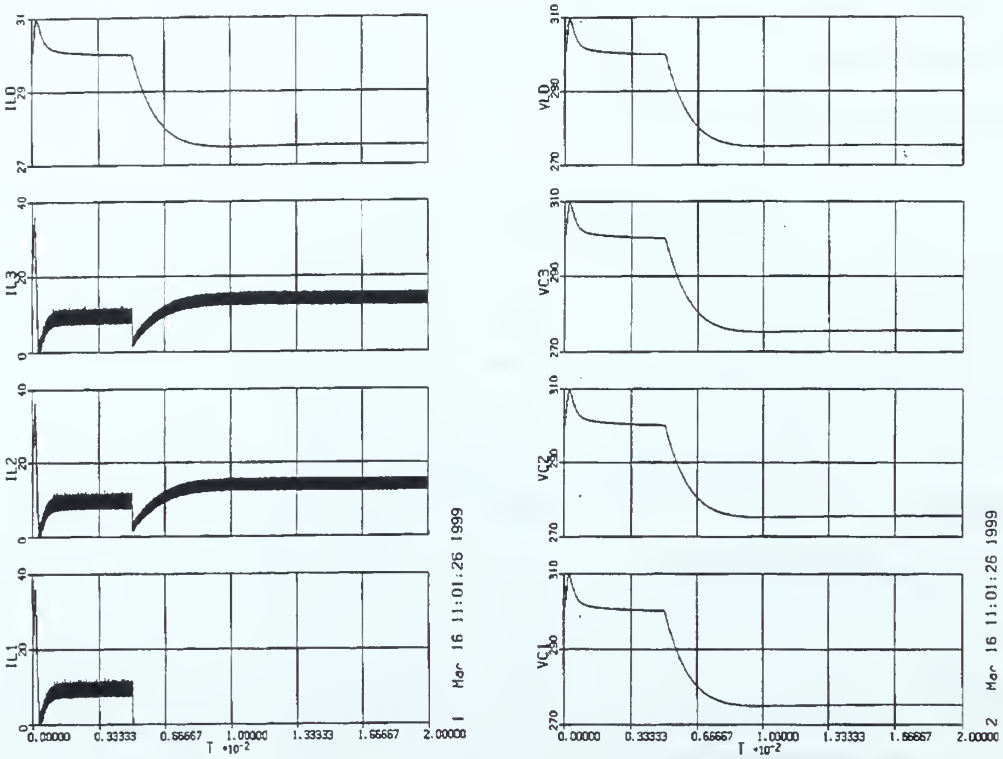


Figure V-6 ASCL Simulation: Three Converters, One Powered Down Abruptly

VI. CONCLUSIONS

A. SUMMARY OF FINDINGS

Current-mode switch control is better suited than PWM for converters with load sharing because of its direct control of output current. Current-mode control is more robust than PWM in that respect.

The rms frequency estimation algorithm and hardware proposed by [24] performs well. The analog model built during research generates an output signal which varies as the actual rms of the input frequencies. One simplifying assumption was that filtering would remove all frequency content except that related to load sharing.

Simulations showed excellent load sharing performance with current-mode frequency-based control, even when controller gains were roughly approximated.

B. FUTURE WORK

Several areas of research related to frequency-based load sharing in the context of PEBB design within DC ZEDS were not fully explored. The following paragraphs outline some of the areas where this research may be continued.

One aspect of frequency-based load sharing not examined was the correlation between perturbation input signal amplitude and perturbation amplitude at the converter output. In order to specify perturbation generator output signal amplitude, filtering of output voltage should be simulated.

The next step in verifying the utility of frequency-based load sharing for DC ZEDS usage should be the construction of a hardware-in-the-loop model. Use of a dSPACE card on a workstation with Simulink allows a controller model to accept inputs from a hardware circuit while the simulation is in progress. Variables from that simulation may also drive outputs back to the hardware circuit. Since all components of a system of converters employing frequency-based load sharing, except the rms frequency estimator circuit itself, are easily simulated, a hardware-in-the-loop test using a frequency estimator circuit in hardware should be much more accurate than a purely digital model.

Controller gains were not precisely calculated for the simulations in this thesis, but were estimated because of the complexity of calculation. Numerical methods such as Newton-Raphson should be considered for precise gain calculation.

One point of difficulty with the two-pole approximation of the multi-pole converter system is that placement of the two poles for slight damping yielded oscillatory response in simulation. The desired response was achieved when the two poles were placed on the real axis. This behavior is most likely caused by the fact that the two-pole system poorly approximates the actual system.

Transient performance simulations in Chapter V Part C showed that the inductor current exhibits a nonminimum phase response—current increases initially before it settles at a lower value. If this behavior remains even in simulations for which precise gains are calculated, a possible solution is the inclusion of a current error term into the expression for i^* (Equation (2-5)), similar to the term $h_i(i_L - i_o)$ in Equation (2-4),. This current error control would effectively provide PID control on converter output voltage v_C and possibly further stabilize current excursions.

APPENDIX A: DERIVATIONS

A. CURRENT-MODE STATE-SPACE DERIVATION

Chapter IV shows a current-mode converter derivation in which the simplifying assumption $i^* = i_L$ is made to justify neglecting the inductor current state variable. A more detailed analysis may require the i_L state variable to be used, especially when slope compensation is employed, since compensation widens the gap between i^* and i_L. The following state-space model development includes i_L in the analysis.

The first task in the derivation is to find a single expression for the duty ratio d in terms of the commanded current i^* and state variables i_L and v_C. As [17] illustrates, inductor current at the start of each switching period, $i_{L\min}$, is expressed by

$$i_{L\min} = i^* - mdT_s \qquad \text{(A-1)}$$

where m is the slope of the rising inductor current plus slope compensation, d is the duty ratio for the switching period in question, and T_s is the switching period. The quantity dT_s represents the time the switch is on. Knowing that i_{Lavg} is equal to i_L at time $(0.5dT_s)$, i_{Lavg} may be expressed as

$$i_{Lavg} = i_{L\min} + \left(\frac{V_{in} - v_C}{L}\right)\frac{dT_s}{2} \qquad \text{(A-2)}$$

or as

$$i_{Lavg} = i^* - mdT_s + \left(\frac{V_{in} - v_C}{L}\right)\frac{dT_s}{2} \qquad \text{(A-3)}$$

when Equations (A-1) and (A-2) are combined.

Slope m is the rising inductor current slope plus slope compensation and may be expressed as

$$m = \frac{V_{in} - v_C}{L} + \frac{v_C}{L}. \qquad \text{(A-4)}$$

Thus the expression for i_{Lavg} may be rewritten as

$$i_{Lavg} = i^* - \frac{V_{in} d T_s}{2L} - \frac{v_C d T_s}{2L} \tag{A-5}$$

Equation (A-5) is the desired expression relating i^*, d, and the state variables i_L and v_C. However, Equation (A-5) is nonlinear. The expression is easily linearized as

$$\Delta i_{Lavg} = \Delta i^* - \left(\frac{V_{in} T_s}{2L}\right)\Delta d - \left(\frac{V_{co} T_s}{2L}\right)\Delta d - \left(\frac{d_o T_s}{2L}\right)\Delta V_{co} \tag{A-6}$$

where V_{co} is the steady-state capacitor voltage, assumed to be equal to V_{ref}, and d_o is the steady-state duty ratio, assumed to be equal to V_{ref} / V_{in}. Of course, since this expression is linearized, the final state-space representation will be linearized as well.

The next task in the derivation is to convert from input Δd to input Δi^* by substituting the expression for Δd into the linearized state-space model. Equation (A-6) is therefore rearranged to solve for Δd.

$$\Delta d = \frac{2L}{\left(V_{in} + V_{ref}\right)T_s}\Delta i^* - \frac{2L}{\left(V_{in} + V_{ref}\right)T_s}\Delta i_{Lavg} - \frac{V_{ref}}{\left(V_{in} + V_{ref}\right)V_{in}}\Delta V_C \tag{A-7}$$

The linearized state-space averaged model for a buck converter power section is

$$\frac{d}{dt}\begin{bmatrix} \Delta v_{C,avg} \\ \Delta i_{L,avg} \end{bmatrix} = \begin{bmatrix} \frac{-1}{RC} & \frac{1}{C} \\ \frac{-1}{L} & 0 \end{bmatrix} \begin{bmatrix} \Delta v_{C,avg} \\ \Delta i_{L,avg} \end{bmatrix} + \begin{bmatrix} 0 \\ \frac{V_{in}}{L} \end{bmatrix} \Delta d \, . \tag{A-8}$$

Equation (A-7) is substituted into Equation (A-8) to replace Δd by Δi^* as the system input. The result is as follows.

$$\frac{d}{dt}\begin{bmatrix} \Delta v_{C,avg} \\ \Delta i_{L,avg} \end{bmatrix} = \begin{bmatrix} \frac{-1}{RC} & \frac{1}{C} \\ \frac{-1}{L} - \frac{V_{ref}}{\left(V_{in} + V_{ref}\right)V_{in}} & \frac{-2V_{in}}{\left(V_{in} + V_{ref}\right)T_s} \end{bmatrix} \begin{bmatrix} \Delta v_{C,avg} \\ \Delta i_{L,avg} \end{bmatrix} + \begin{bmatrix} 0 \\ \frac{2V_{in}}{\left(V_{in} + V_{ref}\right)T_s} \end{bmatrix} \Delta i^* \tag{A-9}$$

The final task in the complete current-mode state-space model derivation is to place a control algorithm into the model and thus convert the model input from Δi^* to ΔV_{ref}. The control algorithm from Equation (2-5) is used, which is expressed by Equations (A-10) and (A-11).

$$\frac{d}{dt}x = V_{ref} - v_C \tag{A-10}$$

$$i^* = h_n x + h_v\left(V_{ref} - v_C\right) \tag{A-11}$$

These equations must be linearized.

$$\frac{d}{dt}\Delta x = \Delta V_{ref} - \Delta v_C \tag{A-12}$$

$$\Delta i^* = h_n \Delta x + h_v\left(\Delta V_{ref} - \Delta v_C\right) \tag{A-13}$$

The final task is completed by adding Equation (A-12) to the state-space model and by substituting Equation (A-13) into the open-loop model input Δi^* in Equation (A-9). The final result is

$$\frac{d}{dt}\begin{bmatrix} \Delta v_{C,avg} \\ \Delta i_{L,avg} \\ \Delta x \end{bmatrix} = \begin{bmatrix} a_{11} & a_{12} & 0 \\ a_{21} & a_{22} & a_{23} \\ -1 & 0 & 0 \end{bmatrix}\begin{bmatrix} \Delta v_{C,avg} \\ \Delta i_{L,avg} \\ \Delta x \end{bmatrix} + \begin{bmatrix} 0 \\ b_2 \\ 1 \end{bmatrix}\Delta V_{ref} \tag{A-14}$$

where

$$a_{11} = \frac{-1}{RC} \tag{A-15}$$

$$a_{12} = \frac{1}{C} \tag{A-16}$$

$$a_{21} = \frac{-1}{L} - \frac{V_{ref}}{\left(V_{in} - V_{ref}\right)V_{in}} - \frac{2V_{in}h_v}{\left(V_{in} - V_{ref}\right)T_s} \tag{A-17}$$

$$a_{22} = \frac{-2V_{in}}{\left(V_{in} - V_{ref}\right)T_s} \tag{A-18}$$

$$a_{23} = \frac{2V_{in}h_n}{\left(V_{in} - V_{ref}\right)T_s} \tag{A-19}$$

and

$$b_2 = \frac{2V_{in}h_v}{\left(V_{in} - V_{ref}\right)T_s}. \tag{A-20}$$

B. OUTPUT CURRENT CONVERSION

The derivation in this section outlines how the converter output current i_o is expressed in terms of state variables, both for the two- and three-converter cases. The two-converter expression is coded into the Matlab state-space representation for two converters, and the three-converter expression is used in the ASCL model.

Recognize from Figure II-1 that converter module output current i_{o1}, according to Ohm's Law, may be expressed as

$$i_{o1} = \frac{v_{C1} - v_{LD}}{R_1} . \tag{A-21}$$

It is useful to derive an expression for load voltage v_{LD} in terms of state variables as an intermediate step in deriving an expression for i_{o1}. Since state-space representations for both two- and three-converter systems are presented in this thesis, the derivations to follow are performed for both cases. The following derivation holds for the power section of any buck converter, regardless of the control method.

1. Load Voltage

a) Two Converters

Kirchhoff's Current Law (KCL) at the node joining two converters to the load gives the following expression.

$$i_{LD} = i_{o1} + i_{o2} \tag{A-22}$$

Simple Ohm's Law expressions for each resistor yield Equations (A-23) to (A-25).

$$i_{o1} = \frac{v_{C1} - v_{LD}}{R_1} \tag{A-23}$$

$$i_{o2} = \frac{v_{C2} - v_{LD}}{R_2} \tag{A-24}$$

$$i_{LD} = \frac{v_{LD}}{R_{LD}} \tag{A-25}$$

The following expression is obtained by substituting these three expressions into Equation (A-22) and solving for load voltage.

$$v_{LD} = v_{C1}\left(\frac{R_2 R_{LD}}{R_1 R_2 + R_1 R_{LD} + R_2 R_{LD}}\right) + v_{C2}\left(\frac{R_1 R_{LD}}{R_1 R_2 + R_1 R_{LD} + R_2 R_{LD}}\right) \tag{A-26}$$

For simplicity, α_2 is defined as

$$\alpha_2 = R_1 R_2 + R_1 R_{LD} + R_2 R_{LD}\,. \tag{A-27}$$

Notice that the subscript "2" indicates that this is the α for a two-converter system and not for module number 2.

Using this definition of α_2, the expression for load voltage may be reduced to

$$v_{LD} = v_{C1}\left(\frac{R_2 R_{LD}}{\alpha_2}\right) + v_{C2}\left(\frac{R_1 R_{LD}}{\alpha_2}\right). \tag{A-28}$$

b) Three Converters

Similar to the two-converter case, KVL at the node joining three converters is

$$i_{LD} = i_{o1} + i_{o2} + i_{o3}\,, \tag{A-29}$$

and may be expanded to

$$\frac{v_{LD}}{R_{LD}} = \frac{v_{C1} - v_{LD}}{R_1} + \frac{v_{C2} - v_{LD}}{R_2} + \frac{v_{C3} - v_{LD}}{R_3}\,. \tag{A-30}$$

By solving for load voltage and isolating capacitor voltage state variables, the following expression is derived

$$v_{LD} = v_{C1}\left(\frac{R_2 R_3 R_{LD}}{\alpha_3}\right) + v_{C2}\left(\frac{R_1 R_3 R_{LD}}{\alpha_3}\right) + v_{C3}\left(\frac{R_1 R_2 R_{LD}}{\alpha_3}\right) \tag{A-31}$$

where

$$\alpha_3 = R_1 R_2 R_3 + R_1 R_2 R_{LD} + R_2 R_3 R_{LD} + R_1 R_3 R_{LD}\,. \tag{A-32}$$

2. Output Current

a) Two Converters

KCL at the node joining two converters gives the equation

$$i_{o1} = i_{LD} - i_{o2}, \tag{A-33}$$

which may be expanded to

$$i_{o1} = \frac{v_{LD}}{R_{LD}} - \frac{v_{C2} - v_{LD}}{R_2}. \tag{A-34}$$

When voltage terms are collected, Equation (A-35) is derived.

$$i_{o1} = v_{LD}\left(\frac{1}{R_{LD}} + \frac{1}{R_2}\right) + v_{C2}\left(\frac{-1}{R_2}\right) \tag{A-35}$$

This equation may be rearranged to yield

$$i_{o1} = v_{LD}\left(\frac{R_2 + R_{LD}}{R_2 R_{LD}}\right) + v_{C2}\left(\frac{-1}{R_2}\right). \tag{A-36}$$

By substituting Equation (A-28) for load voltage into Equation (A-36), the current becomes

$$i_{o1} = v_{C1}\left(\frac{R_2 R_{LD}}{\alpha_2}\right)\left(\frac{R_2 + R_{LD}}{R_2 R_{LD}}\right) + v_{C2}\left(\frac{R_1 R_{LD}}{\alpha_2}\right)\left(\frac{R_2 + R_{LD}}{R_2 R_{LD}}\right) + v_{C2}\left(\frac{-1}{R_2}\right). \tag{A-37}$$

After collecting state variables, Equation (A-37) reduces to

$$i_{o1} = v_{C1}\left(\frac{R_2 + R_{LD}}{\alpha_2}\right) + v_{C2}\left(\frac{R_1 R_2 + R_1 R_{LD} - \alpha_2}{R_2 \alpha_2}\right), \tag{A-38}$$

which may be further simplified to

$$i_{o1} = v_{C1}\left(\frac{R_2 + R_{LD}}{\alpha_2}\right) + v_{C2}\left(\frac{-R_{LD}}{\alpha_2}\right). \tag{A-39}$$

Equation (A-39) is the final expression for i_{o1} in terms of state variables. The expression for i_{o2}, derived in a similar manner, is

$$i_{o2} = v_{C1}\left(\frac{-R_{LD}}{\alpha_2}\right) + v_{C2}\left(\frac{R_1 + R_{LD}}{\alpha_2}\right). \tag{A-40}$$

b) *Three Converters*

The expanded KCL expression at the node joining three converters is

$$i_{o1} = \frac{v_{LD}}{R_{LD}} - \frac{v_{C2} - v_{LD}}{R_2} - \frac{v_{C3} - v_{LD}}{R_3}, \tag{A-41}$$

which may be rearranged as the following when state variables are collected.

$$i_{o1} = v_{LD}\left(\frac{1}{R_{LD}} + \frac{1}{R_2} + \frac{1}{R_3}\right) + v_{C2}\left(\frac{-1}{R_2}\right) + v_{C3}\left(\frac{-1}{R_3}\right) \tag{A-42}$$

Equation (A-42) is converted to the following expression to establish a common denominator.

$$i_{o1} = v_{LD}\left(\frac{R_2R_3 + R_{LD}R_3 + R_{LD}R_2}{R_{LD}R_2R_3}\right) + v_{C2}\left(\frac{-1}{R_2}\right) + v_{C3}\left(\frac{-1}{R_3}\right) \tag{A-43}$$

Just as in the two-converter case, the expression for the load voltage, v_{LD}, from Equation (A-31) is substituted into Equation (A-43). The final expression is simplified when the state variable coefficients are rearranged such that α_3 is in the denominator. The intermediate expressions are quite lengthy but the final result is

$$i_{o1} = v_{C1}\left(\frac{R_2R_3 + R_{LD}R_2 + R_{LD}R_3}{\alpha_3}\right) + v_{C2}\left(\frac{R_{LD}R_3}{\alpha_3}\right) + v_{C3}\left(\frac{R_{LD}R_2}{\alpha_3}\right). \tag{A-44}$$

Expressions for i_{o2} and i_{o3} are derived in a similar manner and are shown in Equations (A-45) and (A-46).

$$i_{o2} = v_{C1}\left(\frac{R_{LD}R_3}{\alpha_3}\right) + v_{C2}\left(\frac{R_1R_3 + R_{LD}R_1 + R_{LD}R_3}{\alpha_3}\right) + v_{C3}\left(\frac{R_{LD}R_1}{\alpha_3}\right) \tag{A-45}$$

$$i_{o3} = v_{C1}\left(\frac{R_{LD}R_2}{\alpha_3}\right) + v_{C2}\left(\frac{R_{LD}R_1}{\alpha_3}\right) + v_{C3}\left(\frac{R_1R_2 + R_{LD}R_1 + R_{LD}R_2}{\alpha_3}\right) \tag{A-46}$$

C. FREQUENCY ERROR CONVERSION

The derivation in this section outlines how estimated frequency ω_{est} is expressed in terms of state variables, both for the two- and three-converter cases. The two-converter expression is used in the Matlab state-space representation, and the three-converter expression is used in the ASCL model.

1. Two Converters

The term $(\omega_{\mathrm{est}} - \omega_{\mathrm{pert}})$ is frequency error, where ω_{est} is the estimated frequency content of the combined output voltage in a multi-converter system, and ω_{pert} is the perturbation frequency of the individual converter corresponding to its own output current i_o. Recall that [24] recommends an rms frequency estimation method, which is also evaluated in this thesis. Recall also that the expression for estimated frequency using the rms method, as given in Equation (3-1), is as follows.

$$\omega_{est} = \frac{\sqrt{c_1^2 \omega_{pert1}^2 + c_2^2 \omega_{pert2}^2 + c_3^2 \omega_{pert3}^2}}{\sqrt{c_1^2 + c_2^2 + c_3^2}} \qquad \text{(A-47)}$$

For the case of two converters, both weighted equally, that expression reduces to

$$\omega_{est} = \frac{\sqrt{\omega_{pert1}^2 + \omega_{pert2}^2}}{\sqrt{2}} \qquad \text{(A-48)}$$

Placing this expression into the state-space representation will introduce nonlinearities. It was realized that when all perturbation frequencies are close, the average is a very good estimate of the rms value. Even though rms frequency estimation was simpler to implement in hardware, estimation by averaging is simpler in state-space modeling and in digital simulation. For that reason, the following expression is considered.

$$\omega_{rms} \cong \omega_{avg} = \frac{\omega_{pert1} + \omega_{pert2}}{2} \qquad \text{(A-49)}$$

Therefore, with ($\omega_{\text{est}} - \omega_{\text{pert}}$) reduced to ($\omega_{\text{avg}} - \omega_{\text{pert}}$), the frequency error term may be expressed as a linear function of state variables.

The perturbation frequency may be expressed as

$$\omega_{pert} = \omega_{\min} + i_o \left(\frac{\omega_{\max} - \omega_{\min}}{i_{orated}} \right) \tag{A-50}$$

where $\omega_{\min}$ and $\omega_{\max}$ are the perturbation frequency range limits, and $i_{\text{o rated}}$ is converter output current associated with its rated power. For simplicity of expression, a constant β is defined and expressed as follows.

$$\beta = \frac{\omega_{\max} - \omega_{\min}}{i_{orated}} \tag{A-51}$$

Thus, Equation (A-50) may be written as

$$\omega_{pert} = \omega_{\min} + i_o \beta . \tag{A-52}$$

Combining Equations (A-49) and (A-52), frequency error for converter one of the two-converter system may be expressed as

$$\left(\omega_{avg} - \omega_{pert1}\right) = \frac{\beta}{2}\left(i_{o2} - i_{o1}\right). \tag{A-53}$$

Finally, by substituting the expressions for i_{o1} and i_{o2} from Equations (A-39) and (A-40) into Equation (A-53), an expression for frequency error in terms of state variables is derived as

$$\left(\omega_{avg} - \omega_{pert1}\right) = \frac{\beta}{2\alpha_2}\left[v_{C1}\left(-R_2 - 2R_{LD}\right) + v_{C2}\left(R_1 + 2R_{LD}\right)\right]. \tag{A-54}$$

Similarly, the frequency error expression for converter two of the two-converter system is

$$\left(\omega_{avg} - \omega_{pert2}\right) = \frac{\beta}{2\alpha_2}\left[v_{C1}\left(R_2 + 2R_{LD}\right) + v_{C2}\left(-R_1 - 2R_{LD}\right)\right]. \tag{A-55}$$

2. Three Converters

The three-converter derivation for frequency error in terms of state variables is quite lengthy but follows the same approach as the two-converter derivation. The starting point is the following expression for average perturbation frequency, similar to Equation (A-49).

$$\omega_{avg} = \frac{\omega_{pert1} + \omega_{pert2} + \omega_{pert3}}{3} \tag{A-56}$$

From Equation (A-56) and the ω_{pert} expression in Equations (A-52), the following expression for frequency error is obtained.

$$\left(\omega_{avg} - \omega_{pert1}\right) = \frac{\beta}{3}\left[-2i_{o1} + i_{o2} + i_{o3}\right] \tag{A-57}$$

Substituting the three i_o expressions of Equations (A-44) to (A-46) into Equation (A-57), the final frequency error is derived.

$$\begin{aligned}\left(\omega_{avg} - \omega_{pert1}\right) = {} & v_{C1}\frac{\beta}{3\alpha_3}\left(-2R_2R_3 - R_{LD}R_2 - R_{LD}R_3\right) \\ & + v_{C2}\frac{\beta}{3\alpha_3}\left(R_1R_3 + 2R_{LD}R_1 - R_{LD}R_3\right) \\ & + v_{C3}\frac{\beta}{3\alpha_3}\left(R_1R_2 + 2R_{LD}R_1 - R_{LD}R_2\right)\end{aligned} \tag{A-58}$$

Similar frequency error expressions may be derived for converters 2 and 3. Those final expressions are given in Equations (A-59) and (A-60).

$$\begin{aligned}\left(\omega_{avg} - \omega_{pert2}\right) = {} & v_{C1}\frac{\beta}{3\alpha_3}\left(R_2R_3 + 2R_{LD}R_2 - R_{LD}R_3\right) \\ & + v_{C2}\frac{\beta}{3\alpha_3}\left(-2R_1R_3 - R_{LD}R_1 - R_{LD}R_3\right) \\ & + v_{C3}\frac{\beta}{3\alpha_3}\left(R_1R_2 + 2R_{LD}R_1 - R_{LD}R_2\right)\end{aligned} \tag{A-59}$$

$$\begin{aligned}\left(\omega_{avg}-\omega_{pert1}\right)=&\, v_{C1}\frac{\beta}{3\alpha_3}\left(R_2R_3+2R_{LD}R_2-R_{LD}R_3\right)\\&+v_{C2}\frac{\beta}{3\alpha_3}\left(R_1R_3+2R_{LD}R_1-R_{LD}R_3\right)\\&+v_{C3}\frac{\beta}{3\alpha_3}\left(-2R_1R_2-R_{LD}R_1-R_{LD}R_2\right)\end{aligned}\qquad\text{(A-60)}$$

APPENDIX B: MATLAB CODE

A. CODE WHICH GENERATED PLOT III-3

```
%  Jonathan Moore
%  Filename:  est.m

%  This routine caluculates the actual rms value of two input
frequencies
%  and generates plots to compare those values with experimentally-
determined
%  values

clear all
format long g

f1 = 2000: 50: 5000;
f2 = 2000: 50: 5000;
w1 = 2*pi*f1;
w2 = 2*pi*f2;
c1 = 1;
c2 = 1;

%  Experimental Data
%    f1 = 2KHz, f2 vs. Vout
f2 = [2000 2500 3000 3500 4000 4500 5000];
w2 = 2*pi*f2;
V1 = [  3  24  46  70  95 119 143]/225;
V2 = [ 43  60  76  97 120 141 165]/225;
V3 = [ 88 102 119 134 153 170 191]/225;
V4 = [135 146 159 172 189 205 225]/225;

e1 = (sqrt((c1^2 * (2*pi*2000).^2) + (c2^2 * w2.^2)) / sqrt(c1^2 +
c2^2));
e2 = (sqrt((c1^2 * (2*pi*3000).^2) + (c2^2 * w2.^2)) / sqrt(c1^2 +
c2^2));
e3 = (sqrt((c1^2 * (2*pi*4000).^2) + (c2^2 * w2.^2)) / sqrt(c1^2 +
c2^2));
e4 = (sqrt((c1^2 * (2*pi*5000).^2) + (c2^2 * w2.^2)) / sqrt(c1^2 +
c2^2));
es1 = (e1 - min(e1))/(.6*max(e4));
es2 = (e2 - min(e1))/(.6*max(e4));
es3 = (e3 - min(e1))/(.6*max(e4));
es4 = (e4 - min(e1))/(.6*max(e4));

ea1 = (2*pi*2000 + w2) / 2;
ea2 = (2*pi*3000 + w2) / 2;
ea3 = (2*pi*4000 + w2) / 2;
ea4 = (2*pi*5000 + w2) / 2;
eas1 = (ea1 - min(ea1))/(.6*max(ea4));
eas2 = (ea2 - min(ea1))/(.6*max(ea4));
eas3 = (ea3 - min(ea1))/(.6*max(ea4));
```

```
eas4 = (ea4 - min(ea1))/(.6*max(ea4));

figure(1);
plot(w2,es1,w2,es2,w2,es3,w2,es4,w2,eas1,'- ',w2,eas2,'- ',w2,eas3,'-
',w2,eas4,'- ',w2,V1,'o',w2,V2,'o',w2,V3,'o',w2,V4,'o'), grid
LEGEND('Theoretical Data, f = 2000','Theoretical Data, f =
3000','Theoretical Data, f = 4000','Theoretical Data, f =
5000','Experimental Data, f = 2000','Experimental Data, f =
3000','Experimental Data, f = 4000','Experimental Data, f = 5000',0)
xlabel('Angular Frequency (rad/sec) Corresponding to f = 2KHz to 5KHz')
ylabel('Frequency Estimator Output, Normalized')
```

B. SINGLE-CONVERTER SYSTEM

```
%  Jonathan Moore
%  Filename:  cm1.m

%  See section on Single-Converter Gain Derivation in Ch IV, Part B

%  This MATLAB code calculates either of the following for a single buck
%  converter using current mode control and no load sharing mechanism.
%    1.  Characteristic polynomial given gains
%    2.  Gains given characteristic polynomial

%  Range of possible load resistance:
%    MIN = 3.33 ohms   (three converters, 100% load)
%    MAX = 100.0 ohms  (one converter, 10% load)

%  Range of possible capacitance:
%    MIN = 400 uF   (one converter)
%    MAX = 1200 uF  (three converters)

clear all
format long g

%  Power section:
R = 33.3;
C = 1200e-6;

%  Specify the desired roots
rdes = [-1000 -800]

%  Find desired polynomial:
pdes = poly(rdes)

b = pdes(2) %8800;
c = pdes(3) %6.4e6;
hv = C*b - (1/R)
hn = c*C

%  Or specify gains:
%hv = 6.95;
%hn = 4800;

A = [ -1/(R*C)-hv/C  hn/C;
```

```
      -1                0 ] ;

B = [ hv/C;  1 ];

pnomial = poly(A);
eigs = eig(A);
```

C. TWO-CONVERTER SYSTEM

```
%  Jonathan Moore
%  Filename:  cm2.m

%  This MATLAB code generates a state-space representation for two
%  current-mode converters using frequency-based load sharing.

%  When gains are known, this model may be used to find eigenvalues
%  (pole locations) and the steady-state values of the state
%  variables.

%  Control defined by the following equations:
%    *  dvC1/dt = (iref1 - io1) / C1
%    *  iref1 = hv1(Vref - vC1 + hf1(west - w1))

%  Assumptions:
%    *  iL = iref
%    *  wrms = wavg

clear all
format short g
%diary p2cm1.out

%  Constants:
P = 9000;              %  rated power
Vin1 = 400;            %  input voltage
Vin2 = 400;
Vref1 = 300;           %  rated voltage
Vref2 = 300;
hv1 = 1.24;            %  1@0.62   2@1.24   3@1.86
hv2 = hv1;
hn1 = 640;             %  1@320    2@640    3@960
hn2 = hn1;
hf1 = 0;
hf2 = hf1;
L1  = 760e-6;
L2  = 760e-6;
C1  = 400e-6;
C2  = 400e-6;
R1  = 0.001;
R2  = 0.001;
RLD  = 10;
wmax = 2*pi*5000;
wmin = 2*pi*2000;
iomax = P/Vref1;
alpha = (R1*R2 + R1*RLD + R2*RLD);
beta = (wmax - wmin)/iomax;
```

```
%  System matrix A ***************
%  row 1:
a11 = (-hv1/C1) + (-hf1*hv1*beta*(-R2-(2*RLD))/(2*C1*alpha)) -
(R2+RLD)/(C1*alpha);
a12 = hn1/C1;
a13 = (-hf1*hn1*beta*(R1+2*RLD)/(2*C1*alpha)) + RLD/(C1*alpha);
a14 = 0;
%  row 2:
a21 = -1 + (hf1*beta*(R2+(2*RLD))/(2*alpha));
a22 = 0;
a23 = -hf1*beta*(R1+(2*RLD))/(2*alpha);
a24 = 0;
%  row 3:
a31 = (-hf2*hn1*beta*(R2+2*RLD)/(2*C2*alpha)) + RLD/(C2*alpha);
a32 = 0;
a33 = (-hv2/C2) + (-hf2*hv2*beta*(-R1-(2*RLD))/(2*C2*alpha)) -
(R1+RLD)/(C2*alpha);
a34 = hn2/C2;
%  row 4:
a41 = -hf2*beta*(R2+(2*RLD))/(2*alpha);
a42 = 0;
a43 = -1 + (hf2*beta*(R1+(2*RLD))/(2*alpha));
a44 = 0;

%x = [ vC1  x1  vC2  x2 ]^T
A = [ a11 a12 a13 a14;
      a21 a22 a23 a24;
      a31 a32 a33 a34;
      a41 a42 a43 a44 ];

%  Input coefficient matrix B *****************
%  column 1:
b11 = hv1/C1;
b21 = 1;
b31 = 0;
b41 = 0;
%  column 2:
b12 = 0;
b22 = 0;
b32 = hv2/C2;
b42 = 1;

u = [ Vref1; Vref2 ];

B = [ b11 b12;
      b21 b22;
      b31 b32;
      b41 b42 ];

EigsOfA = eig(A)
x = -A\B*u;

%diary off
```

APPENDIX C: THREE-CONVERTER ACSL MODEL

A. .CSL FILE

```
!  Jonathan Moore
!  Filename:  cm3.csl
!
!  Three Parallel Converters
!     *  Current mode switching control
!     *  Continuous or discontinuous conduction mode
!     *  Purely resistive load
!     *  Each converter may have different connection resistance
!     *  Each converter may have different reference voltage
!     *  Converter #2 may be powered up or powered down
!  Controller algorithm:
!     *  iLavg ~= iref
!     *  dvC/dt = (iref - io) / C
!     *  iref = hn*x + hv(Vref - vC - hf*(wrms - w)) + ipert
!     *  ipert = Apert * cos(2*pi*wmin*t + phase)
!     *  dx/dt = Vref - vC - hf*(wrms - w)
!______________________________________________________________________

PROGRAM

INITIAL

!  Simulation Parameters
   MAXTERVAL  maxt = 5e-7        !  max step for var step integration
algorithm
                                 !  100 time steps per switching period
   CINTERVAL  cint = 1e-5        !  data communication interval
   ALGORITHM  ialg = 5           !  4 -> RK 2nd, 5 -> RK 4th
   NSTEPS     nstp = 1
   CONSTANT   tstop = 0.05       !  stop point for integration

!  Power Section Parameters
   CONSTANT  P = 9000.           !  Converter Power 9 KW
   CONSTANT  fs1 = 20000.        !  Switching Frequency 20 KHz
   CONSTANT  fs2 = 20000.
   CONSTANT  fs3 = 20000.
   Ts1 = 1/fs1                   !  Switching Period
   Ts2 = 1/fs2
   Ts3 = 1/fs3
   CONSTANT  L1 = 760e-6
   CONSTANT  L2 = 760e-6
   CONSTANT  L3 = 760e-6
   CONSTANT  C1 = 400e-6
   CONSTANT  C2 = 400e-6
   CONSTANT  C3 = 400e-6
   CONSTANT  R1 = 0.02
   CONSTANT  R2 = 0.02
   CONSTANT  R3 = 0.02
   CONSTANT  RLD = 3.33
   CONSTANT  Vdi = 0.0          !  Diode Voltage Drop
   CONSTANT  Vsw = 0.0          !  Switch Voltage Drop
   LOGICAL  SW1on
   LOGICAL  SW2on
   LOGICAL  SW3on
   SW1on = .true.
   SW2on = .true.
   SW3on = .true.

!  Controller Parameters
   CONSTANT  Vref1 = 300.        !  Rated Converter Output Voltage
   CONSTANT  Vref2 = 300.
   CONSTANT  Vref3 = 300.
   CONSTANT  Vin1 = 400.
   CONSTANT  Vin2 = 400.
   CONSTANT  Vin3 = 400.
   CONSTANT  hv1 = 1.96          !  1@0.52  2@1.24   3@1.96
   CONSTANT  hv2 = 1.96
   CONSTANT  hv3 = 1.96
   CONSTANT  hn1 = 960.          !  1@320   2@640    3@960
   CONSTANT  hn2 = 960.
   CONSTANT  hn3 = 960.
   CONSTANT  hf1 = 0.01
   CONSTANT  hf2 = 0.01
   CONSTANT  hf3 = 0.01
   CONSTANT  tau = 0.0001
   CONSTANT  wrmsic = 31396.0
   CONSTANT  pi = 3.14159
   CONSTANT  Apert1 = 0.1
   CONSTANT  Apert2 = 0.1
   CONSTANT  Apert3 = 0.1
   CONSTANT  phase1 = 0.0
   CONSTANT  phase2 = 0.0
   CONSTANT  phase3 = 0.0
   wmin = 2*pi*2000.
   wmax = 2*pi*5000.
   iomax = P/Vref1

!  State Variable Initial Conditions
   CONSTANT  iL1ic = 27.5
   CONSTANT  iL2ic = 27.5
   CONSTANT  iL3ic = 27.5
   CONSTANT  vC1ic = 300.
   CONSTANT  vC2ic = 300.
   CONSTANT  vC3ic = 300.
   CONSTANT  x1ic = 0.049
   CONSTANT  x2ic = 0.049
   CONSTANT  x3ic = 0.049

!  Continuous Conduction Mode
   LOGICAL ccm1
   LOGICAL ccm2
   LOGICAL ccm3
   ccm1 = .true.
   ccm2 = .true.
   ccm3 = .true.
```

```
END !initial

DYNAMIC

   TERMT (t .GE. (tstop-0.5*cint))

   DERIVATIVE

!Vin1 = Vin1a + 10.0*sin(5000.0*t)

!      Control Algorithm
       px1 = Vref1 - vC1 + hf1*(wrms - w1)
       px2 = Vref2 - vC2 + hf2*(wrms - w2)
       px3 = Vref3 - vC3 + hf3*(wrms - w3)
       x1 = INTEG(px1, x1ic)
       x2 = INTEG(px2, x2ic)
       x3 = INTEG(px3, x3ic)
       i1pert = Apert1 * cos(2*pi*wmin*t + phase1)
       i2pert = Apert2 * cos(2*pi*wmin*t + phase2)
       i3pert = Apert3 * cos(2*pi*wmin*t + phase3)
       i1ref = hn1*x1 + hv1*(px1) + i1pert
       i2ref = hn2*x2 + hv2*(px2) + i2pert
       i3ref = hn3*x3 + hv3*(px3) + i3pert

!      Reference Current Ramp with Slope Compensation -- switch drop
ignored
       i1ramp = (vC1/L1)*mod(t,Ts1)
       i2ramp = (vC2/L2)*mod(t,Ts2)
       i3ramp = (vC3/L3)*mod(t,Ts3)
       i1comp = iL1 + i1ramp
       i2comp = iL2 + i2ramp
       i3comp = iL3 + i3ramp

!      Frequency Injection
       beta = (wmax - wmin)/iomax
       w1 = wmin + io1*beta
       w2 = wmin + io2*beta
       w3 = wmin + io3*beta
       wi = SQRT(w1**2 + w2**2 + w3**2)/SQRT(3.)
       wrms = REALPL(tau,wi,wrmsic)

!      Determine if Switch 1 is ON or OFF
       PROCEDURAL(SW1on,isw1 = i1comp,i1ref,iL1)
          IF (i1ref .GT. i1comp) THEN
             SW1on = .true.
             isw1 = iL1
          ELSE
             SW1on = .false.
             isw1 = 0.0
          ENDIF
       END !procedural

!      Determine if Switch 2 is ON or OFF
       PROCEDURAL(SW2on,isw2 = i2comp,i2ref,iL2)
          IF (i2ref .GT. i2comp) THEN
             SW2on = .true.
```

```
            isw2 = iL2
         ELSE
            SW2on = .false.
            isw2 = 0.0
         ENDIF
      END !procedural

!     Determine if Switch 3 is ON or OFF
      PROCEDURAL(SW3on,isw3 = i3comp,i3ref,iL3)
         IF (i3ref .GT. i3comp) THEN
            SW3on = .true.
            isw3 = iL3
         ELSE
            SW3on = .false.
            isw3 = 0.0
         ENDIF
      END !procedural

!     Derivative of Inductor 1 Current:  v = L di/dt
      PROCEDURAL(piL1 = SW1on,ccm1,Vin1,vC1,Vdi,Vsw,L1)
         IF (SW1on) THEN
            ccm1 = .true.
            piL1 = (Vin1-Vsw-vC1)/L1
         ELSE
            IF (ccm1) THEN
               piL1 = (-Vdi-vC1)/L1
            ELSE
               piL1 = 0.0    !"discontinuous conduction mode"
            ENDIF
         ENDIF
      END !procedural

!     Derivative of Inductor 2 Current:  v = L di/dt
      PROCEDURAL(piL2 = SW2on,ccm2,Vin2,vC2,Vdi,Vsw,L2)
         IF (SW2on) THEN
            ccm2 = .true.
            piL2 = (Vin2-Vsw-vC2)/L2
         ELSE
            IF (ccm2) THEN
               piL2 = (-Vdi-vC2)/L2
            ELSE
               piL2 = 0.0    ! discontinuous conduction mode
            ENDIF
         ENDIF
      END !procedural

!     Derivative of Inductor 3 Current:  v = L di/dt
      PROCEDURAL(piL3 = SW3on,ccm3,Vin3,vC3,Vdi,Vsw,L3)
         IF (SW3on) THEN
            ccm3 = .true.
            piL3 = (Vin3-Vsw-vC3)/L3
         ELSE
            IF (ccm3) THEN
               piL3 = (-Vdi-vC3)/L3
            ELSE
               piL3 = 0.0    ! discontinuous conduction mode
            ENDIF
         ENDIF
      END !procedural

!     Derivative of Capacitor Voltage:  i = C dv/dt
      pvC1 = (iL1 - io1)/C1
      pvC2 = (iL2 - io2)/C2
      pvC3 = (iL3 - io3)/C3

!     State Variables
      iL1ub = INTEG(piL1, iL1ic)
      iL2ub = INTEG(piL2, iL2ic)
      iL3ub = INTEG(piL3, iL3ic)
      iL1 = BOUND(0.0, 1.0e6, iL1ub)
      iL2 = BOUND(0.0, 1.0e6, iL2ub)
      iL3 = BOUND(0.0, 1.0e6, iL3ub)
      vC1 = INTEG(pvC1, vC1ic)
      vC2 = INTEG(pvC2, vC2ic)
      vC3 = INTEG(pvC3, vC3ic)

!     Discontinuous Conduction Mode when iL tries to go neg
      SCHEDULE  dcm1 .XN. iL1
      SCHEDULE  dcm2 .XN. iL2
      SCHEDULE  dcm3 .XN. iL3

!     Power Section Dynamics
      alpha = R1*R2*R3 + R1*R2*RLD + R2*R3*RLD + R1*R3*RLD
      vLD = vC1*(R2*R3*RLD/alpha) + vC2*(R1*R3*RLD/alpha) &
           + vC3*(R1*R2*RLD/alpha)
      io1 = vLD*(1./RLD + 1./R2 + 1./R3) - vC2/R2 - vC3/R3
      io2 = vLD*(1./RLD + 1./R1 + 1./R3) - vC1/R1 - vC3/R3
      io3 = vLD*(1./RLD + 1./R1 + 1./R2) - vC1/R1 - vC2/R2
      iLD = io1 + io2 + io3

!     Converter Output Power
      S1 = vC1 * io1
      S2 = vC2 * io2
      S3 = vC3 * io3
      SLD = vLD * iLD

   END !derivative

   DISCRETE dcm1  ! discontinuous conduction mode
      ccm1 = .false.
      iLub1 = 0.0
   END !discrete

   DISCRETE dcm2  ! discontinuous conduction mode
      ccm2 = .false.
      iLub2 = 0.0
   END !discrete

   DISCRETE dcm3  ! discontinuous conduction mode
      ccm3 = .false.
      iLub3 = 0.0
   END !discrete

END  !dynamic
END  !program
```

B. .CMD FILE

```
!  Jonathan Moore
!  Filename:  cm3.cmd

!  Command file for ACSL simulation of three parallel current-mode buck
!  converters using frequency-based load sharing.

s strplt = .t.     !  one variable per x-axis
s calplt = .f.
s plt = 1
s devplt = 1       !  5 -> ps
                   !  1 -> graphic desplay
s ppoplt = .f.     !  true rotates plot 90 deg
s xinspl = 6       !  x-axis plot units
s weditg = .f.     !  false suppresses data write each time SCHEDULE
occurs
s nrwitg = .f.     !  true enables accumulation of data after a CONTIN
s alcplt = .f.     !  false for b&w plots

prepare
t,iL1,iL2,iL3,vC1,vC2,vC3,x1,x2,x3,io1,io2,io3,vLD,iLD,w1,w2,w3,wi,wrms
prepare Vin1,Vin2,Vin3,isw1,isw2,isw3,i1ref,i2ref,iref3,i1comp,i2comp
prepare S1,S2,S3,SLD,i1pert,i2pert,i3pert,Vref1,Vref2,Vref3

!****************************** NOTE *****************************
!  each of these procedures performs best when it is the first
!  after starting acsl

!*********************************************************************
!  First study:  steady state conditions, unequal connection resistances
proced one
  s tstop = 0.01
  s R1 = 0.02
  s R2 = 0.04
  s R3 = 0.05
  start
  s plt = 1
  s devplt = 5
  plot /lo=0 /hi=40 il1,il2,il3,vld /hi=400
  s tstop = 0.1
  s hf1 = 0.0
  s hf2 = 0.0
  s hf3 = 0.0
  start
  s plt = 2
  plot /lo=0 /hi=40 il1, /hi=60 il2,il3,vld /hi=400
end

!*********************************************************************
!  Second study:  steady state conditions, unequal reference voltages
proced two
```

```
  s tstop = 0.02
  s Vref1 = 280.
  s Vref2 = 300.
  s Vref3 = 320.
  start
  s plt = 3
  s devplt = 5
  plot il1,il2,il3,vld
  s hf1 = 0
  s hf2 = 0
  s hf3 = 0
  start
  s plt = 4
  plot il1,il2,il3,vld
end

!**********************************************************************
!  Third study:  step change in load from 100% to 20% rated load with
three
!  converters online.
proced down
  s tstop = 0.005
  s RLD = 3.33         !  100% load for 3 converters
  start
  s devplt = 5
  s nrwitg = .true.
  s tstop = 0.02
  s RLD = 16.67        !  20% load for 3 converters
  contin
  s nrwitg = .false.
  s plt = 10
  plot /lo=0 /hi=60 il1,il2,il3,ild /hi=120
!  pause
  s plt = 11
  plot vc1,vc2,vc3,vld
end

!**********************************************************************
!  step from 100% to 20% load
proced up
  s tstop = 0.005
  s RLD = 16.67        !  20% load for 3 converters
  s iL1ic = 3.8
  s il2ic = 3.8
  s il3ic = 3.8
  s vC1ic = 300.
  s vc2ic = 300.
  s vc3ic = 300.
  s x1ic = 0.0239
  s x2ic = 0.0239
  s x3ic = 0.0239
  s wrmsic = 16349.
  start
  s nrwitg = .true.
  s tstop = 0.01
  s RLD = 3.33         !  100% load for 3 converters
  contin
  s nrwitg = .false.
end

!************************************************************************
proced on
  s RLD = 10.
  s Vin1 = 0.
  s iL1ic = 0.
  s iL2ic = 13.49
  s iL3ic = 13.49
  s vC1ic = 275.4
  s vC2ic = 275.4
  s vC3ic = 275.4
  s x1ic = 9.06
  s x2ic = 0.028
  s x3ic = 0.028
  s wrmsic = 18782.5
  s tstop = 0.005
  start
  s Vin1 = 400.
  s tstop = 0.01
  s nrwitg = .true.
  contin
  s nrwitg = .false.
!  s plt = 12
!  s devplt = 5
  plot il1,il2,il3,ild
  pause
!  s plt = 13
  plot vc1,vc2,vc3,vld
end

!************************************************************************
!  Fourth study:  three converters online, one is powered down abruptly
proced off
  s RLD = 10.
  s iL1ic = 19.5
  s iL2ic = 19.5
  s iL3ic = 19.5
  s vC1ic = 300.
  s vC2ic = 300.
  s vC3ic = 300.
  s x1ic = 0.03
  s x2ic = 0.03
  s x3ic = 0.03
  s wrmsic = 25116.8
  s tstop = 0.005
  start
  s Vin1 = 0.
  s tstop = 0.02
  s nrwitg = .true.
  contin
  s nrwitg = .false.
  s plt = 12
  s devplt = 5
  plot il1,il2,il3,ild
!  pause
```

```
  s plt = 13
  plot vc1,vc2,vc3,v1d
end
```

APPENDIX D: DATA SHEETS

AD536A TRUE RMS-TO-DC CONVERTER

ANALOG DEVICES

Integrated Circuit, True RMS-to-DC Converter

AD536A

FEATURES

True RMS-to-DC Conversion

Laser-Trimmed to High Accuracy
- 0.2% max Error (AD536AK)
- 0.5% max Error (AD536AJ)

Wide Response Capability:
- Computes RMS of AC and DC Signals
- 450 kHz Bandwidth: V rms > 100 mV
- 2 MHz Bandwidth: V rms > 1 V
- Signal Crest Factor of 7 for 1% Error

dB Output with 60 dB Range

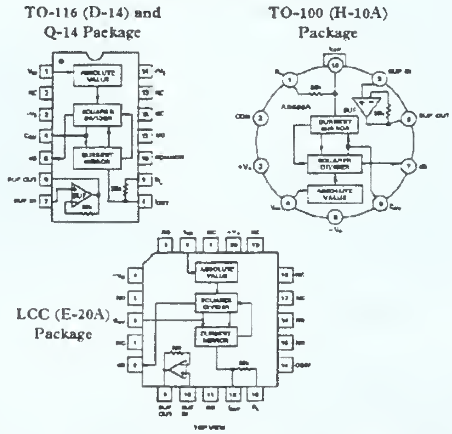
Low Power: 1.2 mA Quiescent Current

Single or Dual Supply Operation

Monolithic Integrated Circuit

–55°C to +125°C Operation (AD536AS)

PIN CONFIGURATIONS AND FUNCTIONAL BLOCK DIAGRAMS



PRODUCT DESCRIPTION

The AD536A is a complete monolithic integrated circuit which performs true rms-to-dc conversion. It offers performance which is comparable or superior to that of hybrid or modular units costing much more. The AD536A directly computes the true rms value of any complex input waveform containing ac and dc components. It has a crest factor compensation scheme which allows measurements with 1% error at crest factors up to 7. The wide bandwidth of the device extends the measurement capability to 300 kHz with 3 dB error for signal levels above 100 mV.

An important feature of the AD536A not previously available in rms converters is an auxiliary dB output. The logarithm of the rms output signal is brought out to a separate pin to allow the dB conversion, with a useful dynamic range of 60 dB. Using an externally supplied reference current, the 0 dB level can be conveniently set by the user to correspond to any input level from 0.1 to 2 volts rms.

The AD536A is laser trimmed at the wafer level for input and output offset, positive and negative waveform symmetry (dc reversal error), and full-scale accuracy at 7 V rms. As a result, no external trims are required to achieve the rated accuracy of the unit.

There is full protection for both inputs and outputs. The input circuitry can take overload voltages well beyond the supply levels. Loss of supply voltage with inputs connected will not cause unit failure. The output is short-circuit protected.

The AD536A is available in two accuracy grades (J, K) for commercial temperature range (0°C to +70°C) applications, and one grade (S) rated for the –55°C to +125°C extended range. The AD536AK offers a maximum total error of ±2 mV ±0.2% of reading, and the AD536AJ and AD536AS have maximum errors of ±5 mV ±0.5% of reading. All three versions are available in either a hermetically sealed 14-pin DIP or 10-pin TO-100 metal can. The AD536AS is also available in a 20-pin hermetically sealed ceramic leadless chip carrier

PRODUCT HIGHLIGHTS

1. The AD536A computes the true root-mean-square level of a complex ac (or ac plus dc) input signal and gives an equivalent dc output level. The true rms value of a waveform is a more useful quantity than the average rectified value since it relates directly to the power of the signal. The rms value of a statistical signal also relates to its standard deviation.
2. The crest factor of a waveform is the ratio of the peak signal swing to the rms value. The crest factor compensation scheme of the AD536A allows measurement of highly complex signals with wide dynamic range.
3. The only external component required to perform measurements to the fully specified accuracy is the capacitor which sets the averaging period. The value of this capacitor determines the low frequency ac accuracy, ripple level and settling time.
4. The AD536A will operate equally well from split supplies or a single supply with total supply levels from 5 to 36 volts. The one milliampere quiescent supply current makes the device well-suited for a wide variety of remote controllers and battery powered instruments.
5. The AD536A directly replaces the AD536 and provides improved bandwidth and temperature drift specifications.

REV. A

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Tel: 617/329-4700 Fax: 617/326-8703

AD536A–SPECIFICATIONS (@ +25°C, and ±15 V dc unless otherwise noted)

Model	AD536AJ			AD536AK			AD536AS			
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
TRANSFER FUNCTION		$V_{OUT} = \sqrt{avg.(V_{IN})^2}$			$V_{OUT} = \sqrt{avg.(V_{IN})^2}$			$V_{OUT} = \sqrt{avg.(V_{IN})^2}$		
CONVERSION ACCURACY										
Total Error, Internal Trim[1] (Figure 1)			±5 ±0.5			±2 ±0.2			±5 ±0.5	mV ± % of Reading
vs. Temperature, T_{MIN} to +70°C			±0.1 ±0.01			±0.05 ±0.005			±0.1 ±0.005	mV ± % of Reading/°C
+70°C to +125°C									±0.3 ±0.005	mV ± % of Reading/°C
vs. Supply Voltage		±0.1 ±0.01			±0.1 ±0.01			±0.1 ±0.01		mV ± % of Reading/V
dc Reversal Error		±0.2			±0.1			±0.2		± % of Reading
Total Error, External Trim[1] (Figure 2)		±3 ±0.3			±2 ±0.1			±3 ±0.3		mV ± % of Reading
ERROR VS. CREST FACTOR[2]										
Crest Factor 1 to 2		Specified Accuracy			Specified Accuracy			Specified Accuracy		
Crest Factor = 3		-0.1			0.1			-0.1		% of Reading
Crest Factor = 7		-1.0			-1.0			-1.0		% of Reading
FREQUENCY RESPONSE[3]										
Bandwidth for 1% Additional Error (0.09 dB)										
V_{IN} = 10 mV		5			5			5		kHz
V_{IN} = 100 mV		45			45			45		kHz
V_{IN} = 1 V		120			120			120		kHz
±3 dB Bandwidth										
V_{IN} = 10 mV		90			90			90		kHz
V_{IN} = 100 mV		450			450			450		kHz
V_{IN} = 1 V		2.3			2.3			2.3		MHz
AVERAGING TIME CONSTANT (Figure 5)		25			25			25		ms/µF CAV
INPUT CHARACTERISTICS										
Signal Range, ±15 V Supplies										
Continuous rms Level		0 to 7			0 to 7			0 to 7		V rms
Peak Transient Input			±20			±20			±20	V peak
Continuous rms Level, ±5 V Supplies		0 to 2			0 to 2			0 to 2		V rms
Peak Transient Input, ±5 V Supplies			±7			±7			±7	V peak
Maximum Continuous Nondestructive Input Level (All Supply Voltages)			±25			±25			±25	V peak
Input Resistance	13.33	16.67	20	13.33	16.67	20	13.33	16.67	20	kΩ
Input Offset Voltage		0.8	±2		0.5	±1		0.8	±2	mV
OUTPUT CHARACTERISTICS										
Offset Voltage, V_{IN} = COM (Figure 1)		±1	±2		±0.5	±1			±2	mV
vs. Temperature		±0.1			±0.1				±0.2	mV/°C
vs. Supply Voltage		±0.1			±0.1			±0.2		mV/V
Voltage Swing, ±15 V Supplies	0 to +11	+12.5		0 to +11	+12.5		0 to +11	+12.5		V
±5 V Supply	0 to +2			0 to +2			0 to +2			V
dB OUTPUT (Figure 13)										
Error, V_{IN} 7 mV to 7 V rms, 0 dB = 1 V rms		±0.4	±0.6		±0.2	±0.3		±0.5	±0.6	dB
Scale Factor		-3			-3			-3		mV/dB
Scale Factor TC (Uncompensated, see Figure 1 for Temperature Compensation)		-0.033			-0.033			-0.033		dB/°C
		+0.33			+0.33			+0.33		% of Reading/°C
I_{REF} for 0 dB = 1 V rms	5	20	80	5	20	80	5	20	80	µA
I_{REF} Range	1		100	1		100	1		100	µA
I_{OUT} TERMINAL										
I_{OUT} Scale Factor		40			40			40		µA/V rms
I_{OUT} Scale Factor Tolerance		±10	±20		±10	±20		±10	±20	%
Output Resistance	20	25	30	20	25	30	20	25	30	kΩ
Voltage Compliance		$-V_S$ to ($+V_S$ −2.5 V)			$-V_S$ to ($+V_S$ −2.5 V)			$-V_S$ to ($+V_S$ −2.5 V)		V
BUFFER AMPLIFIER										
Input and Output Voltage Range	V_S to ($+V_S$ −2.5 V)			$-V_S$ to ($+V_S$ −2.5 V)			$-V_S$ to ($+V_S$ −2.5 V)			V
Input Offset Voltage, R_S = 25 k		±0.5	±4		±0.5	±4		±0.5	±4	mV
Input Bias Current		20	60		20	60		20	60	nA
Input Resistance		10^8			10^8			10^8		Ω
Output Current	(+5 mA, −130 µA)			(+5 mA, −130 µA)			(+5 mA, −130 µA)			
Short Circuit Current		20			20			20		mA
Output Resistance			0.5			0.5			0.5	Ω
Small Signal Bandwidth		1			1			1		MHz
Slew Rate[4]		5			5			5		V/µs
POWER SUPPLY										
Voltage Rated Performance		±15			±15			±15		V
Dual Supply	±3.0		±18	±3.0		±18	±3.0		±18	V
Single Supply	+5		+36	+5		+36	+5		+36	V
Quiescent Current										
Total V_S, 5 V to 36 V, T_{MIN} to T_{MAX}		1.2	2		1.2	2		1.2	2	mA
TEMPERATURE RANGE										
Rated Performance	0		+70	0		+70	-55		+125	°C
Storage	-55		+150	-55		+150	-55		+150	°C
NUMBER OF TRANSISTORS		65			65			65		
PACKAGE OPTIONS										
Ceramic DIP (D-14)		AD536AJD			AD536AKD			AD536ASH		
Metal Can TO-100 (H-10A)		AD5536AJH			AD536AKH			AD536ASH		
LCC (E-20A)								AD536ASE		

NOTES

[1] Accuracy is specified for 0 V to 7 V rms, dc or 1 kHz sine wave input with the AD536A connected as in the figure referenced

[2] Error vs. crest factor is specified as an additional error for 1 V rms rectangular pulse input, pulse width = 200 µs.

[3] Input voltages are expressed in volts rms, and error is percent of reading.

[4] With 2k external pull-down resistor.

Specifications subject to change without notice

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage
 Dual Supply . . . . ±18 V
 Single Supply . . . . +36 V
Internal Power Dissipation[2] . . . . 500 mW
Maximum Input Voltage . . . . ±25 V Peak
Buffer Maximum Input Voltage . . . . ±V_S
Maximum Input Voltage . . . . ±25 V Peak
Storage Temperature Range . . . . –55°C to +150°C
Operating Temperature Range
 AD536AJ/K . . . . 0°C to +70°C
 AD536AS . . . . 55°C to +125°C
Lead Temperature Range
 (Soldering 60 sec) . . . . +300°C
ESD Rating . . . . 1000 V

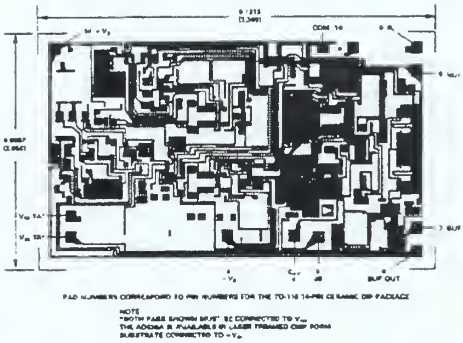
NOTES

[1] Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2] 10-Pin Header: θ_{JA} = 150°C/W
20-Pin LCC: θ_{JA} = 95°C/W
14-Pin Size Brazed Ceramic DIP: θ_{JA} = 95°C/W

CHIP DIMENSIONS AND PAD LAYOUT

Dimensions shown in inches and (mm).



ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD536AJD	0°C to +70°C	Side Brazed Ceramic DIP	D-14
AD536AKD	0°C to +70°C	Side Brazed Ceramic DIP	D-14
AD536AJH	0°C to +70°C	Header	H-10A
AD536AKH	0°C to +70°C	Header	H-10A
AD536AJQ	0°C to +70°C	Cerdip	Q-14
AD536AKQ	0°C to +70°C	Cerdip	Q-14
AD536ASD	–55°C to +125°C	Side Brazed Ceramic DIP	D-14
AD536ASD/883B	–55°C to +125°C	Side Brazed Ceramic DIP	D-14
AD536ASE	–55°C to +125°C	LCC	E-20A
AD536ASE/883B	–55°C to +125°C	LCC	E-20A
AD536ASH	–55°C to +125°C	Header	H-10A
AD536ASH/883B	–55°C to +125°C	Header	H-10A

NOTE

[1] "S" grade chips are available tested at +25°C and +125°C. "J" grade chips are also available.

STANDARD CONNECTION

The AD536A is simple to connect for the majority of high accuracy rms measurements, requiring only an external capacitor to set the averaging time constant. The standard connection is shown in Figure 1. In this configuration, the AD536A will measure the rms of the ac and dc level present at the input, but will show an error for low frequency inputs as a function of the filter capacitor, C_{AV}, as shown in Figure 5. Thus, if a 4 µF capacitor is used, the additional average error at 10 Hz will be 0.1%, at 3 Hz it will be 1%. The accuracy at higher frequencies will be according to specification. If it is desired to reject the dc input, a capacitor is added in series with the input, as shown in Figure 3, the capacitor must be nonpolar. If the AD536A is driven with power supplies with a considerable amount of high frequency ripple, it is advisable to bypass both supplies to ground with 0.1 µF ceramic discs as near the device as possible

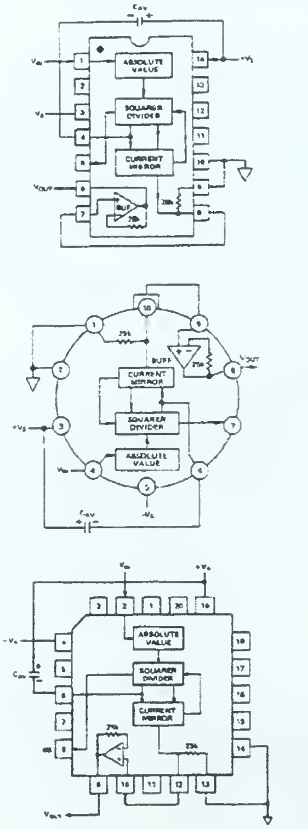


Figure 1. Standard RMS Connection

The input and output signal ranges are a function of the supply voltages; these ranges are shown in Figure 14. The AD536A can also be used in an unbuffered voltage output mode by disconnecting the input to the buffer. The output then appears unbuffered across the 25k resistor. The buffer amplifier can then be used for other purposes. Further the AD536A can be used in a current output mode by disconnecting the 25k resistor from ground. The output current is available at Pin 8 (Pin 10 on the "H" package) with a nominal scale of 40 µA per volt rms input positive out.

OPTIONAL EXTERNAL TRIMS FOR HIGH ACCURACY

If it is desired to improve the accuracy of the AD536A, the external trims shown in Figure 2 can be added. R4 is used to trim the offset. Note that the offset trim circuit adds 365 Ω in series with the internal 25 kΩ resistor. This will cause a 1.5% increase in scale factor, which is trimmed out by using R1 as shown. Range of scale factor adjustment is ±1.5%.

The trimming procedure is as follows:

1. Ground the input signal, V_{IN}, and adjust R4 to give zero volts output from Pin 6. Alternatively, R4 can be adjusted to give the correct output with the lowest expected value of V_{IN}.
2. Connect the desired full scale input level to V_{IN}, either dc or a calibrated ac signal (1 kHz is the optimum frequency); then trim R1, to give the correct output from Pin 6, i.e., 1000 V dc input should give 1.000 V dc output. Of course, a ±1.000 V peak-to-peak sine wave should give a 0.707 V dc output. The remaining errors, as given in the specifications are due to the nonlinearity.

The major advantage of external trimming is to optimize device performance for a reduced signal range; the AD536A is internally trimmed for a 7 V rms full-scale range

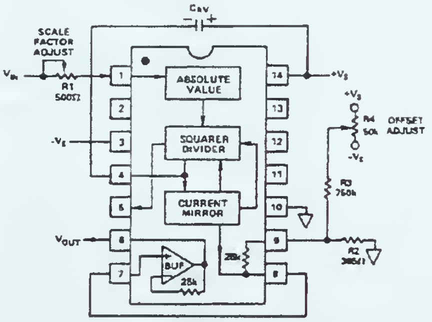


Figure 2. Optional External Gain and Output Offset Trims

SINGLE SUPPLY CONNECTION

The applications in Figures 1 and 2 require the use of approximately symmetrical dual supplies. The AD536A can also be used with only a single positive supply down to +5 volts, as shown in Figure 3. The major limitation of this connection is that only ac signals can be measured since the differential input stage must be biased off ground for proper operation. This biasing is done at Pin 10; thus it is critical that no extraneous signals be coupled into this point. Biasing can be accomplished by using a resistive divider between $+V_S$ and ground. The values of the resistors can be increased in the interest of lowered power consumption, since only 5 mA of current flows into Pin 10 (Pin 2 on the "H" package). AC input coupling requires only capacitor C2 as shown; a dc return is not necessary as it is provided internally. C2 is selected for the proper low frequency break point with the input resistance of 16.7 kΩ; for a cutoff at 10 Hz, C2 should be 1 µF. The signal ranges in this connection are slightly more restricted than in the dual supply connection. The input and output signal ranges are shown in Figure 14. The load resistor, R_L, is necessary to provide output sink current.

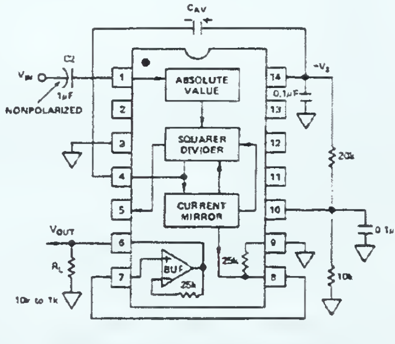


Figure 3. Single Supply Connection

CHOOSING THE AVERAGING TIME CONSTANT

The AD536A will compute the rms of both ac and dc signals. If the input is a slowly-varying dc signal, the output of the AD536A will track the input exactly. At higher frequencies, the average output of the AD536A will approach the rms value of the input signal. The actual output of the AD536A will differ from the ideal output by a dc (or average) error and some amount of ripple, as demonstrated in Figure 4.

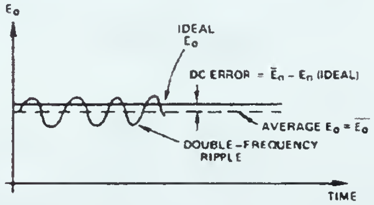


Figure 4. Typical Output Waveform for Sinusoidal Input

The dc error is dependent on the input signal frequency and the value of C_{AV}. Figure 5 can be used to determine the minimum value of C_{AV} which will yield a given percent dc error above a given frequency using the standard rms connection.

The ac component of the output signal is the ripple. There are two ways to reduce the ripple. The first method involves using a large value of C_{AV}. Since the ripple is inversely proportional to C_{AV}, a tenfold increase in this capacitance will affect a tenfold reduction in ripple. When measuring waveforms with high crest factors, (such as low duty cycle pulse trains), the averaging time constant should be at least ten times the signal period. For example, a 100 Hz pulse rate requires a 100 ms time constant, which corresponds to a 4 µF capacitor (time constant = 25 ms per µF).

The primary disadvantage in using a large C_{AV} to remove ripple is that the settling time for a step change in input level is increased proportionately. Figure 5 shows that the relationship between C_{AV} and 1% settling time is 115 milliseconds for each microfarad of C_{AV}. The settling time is twice as great for decreasing signals as for increasing signals (the values in Figure 5 are for decreasing signals). Settling time also increases for low signal levels, as shown in Figure 6.

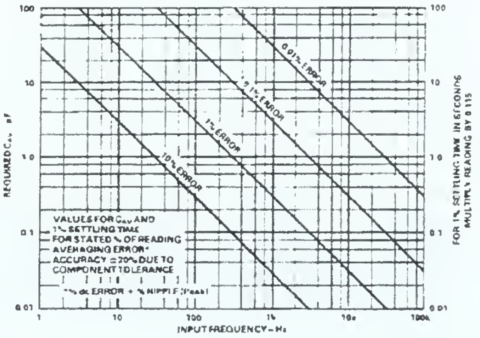


Figure 5. Error/Settling Time Graph for Use with the Standard rms Connection in Figure 1

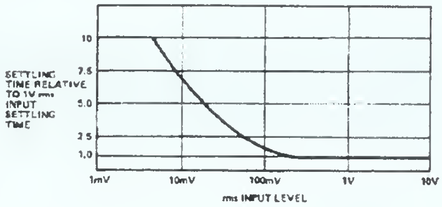


Figure 6. Settling Time vs. Input Level

A better method for reducing output ripple is the use of a "post-filter." Figure 7 shows a suggested circuit. If a single-pole filter is used (C3 removed, R_X shorted), and C2 is approximately twice the value of C_{AV}, the ripple is reduced as shown in Figure 8 and settling time is increased. For example, with C_{AV} = 1 µF and C2 = 2.2 µF, the ripple for a 60 Hz input is reduced from 10% of reading to approximately 0.3% of reading. The settling time, however, is increased by approximately a factor of 3. The values of C_{AV} and C2, can, therefore, be reduced to permit faster settling times while still providing substantial ripple reduction.

The two-pole post-filter uses an active filter stage to provide even greater ripple reduction without substantially increasing the settling times over a circuit with a one-pole filter. The values of C_{AV}, C2, and C3 can then be reduced to allow extremely fast settling times for a constant amount of ripple. Caution should be exercised in choosing the value of C_{AV}, since the dc error is dependent upon this value and is independent of the post filter.

For a more detailed explanation of these topics refer to the *RMS to DC Conversion Application Guide 2nd Edition,* available from Analog Devices.

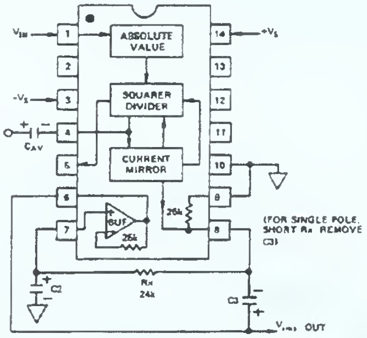


Figure 7. 2-Pole "Post" Filter

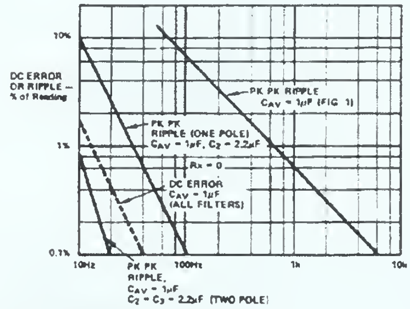


Figure 8. Performance Features of Various Filter Types

AD536A PRINCIPLE OF OPERATION

The AD536A embodies an implicit solution of the rms equation that overcomes the dynamic range as well as other limitations inherent in a straightforward computation of rms. The actual computation performed by the AD536A follows the equation:

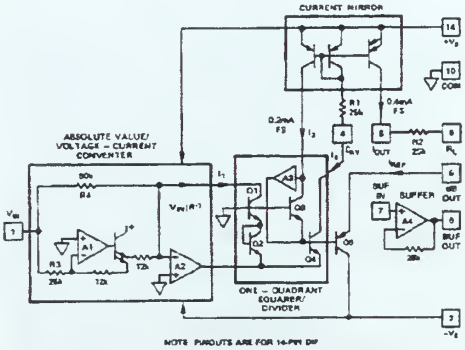
$$V\,rms = Avg.\left[\frac{V_{IN}^{\,2}}{V\,rms}\right]$$

Figure 9 is a simplified schematic of the AD536A; it is subdivided into four major sections: absolute value circuit (active rectifier), squarer/divider, current mirror, and buffer amplifier. The input voltage, V_{IN}, which can be ac or dc, is converted to a unipolar current I_1, by the active rectifier A_1, A_2. I_1 drives one input of the squarer/divider, which has the transfer function:

$$I_4 = I_1^2/I_3$$

The output current, I_4, of the squarer/divider drives the current mirror through a low-pass filter formed by R1 and the externally connected capacitor, C_{AV}. If the R1, C_{AV} time constant is much greater than the longest period of the input signal, then I_4 is effectively averaged. The current mirror returns a current I_3, which equals Avg. $[I_4]$, back to the squarer/divider to complete the implicit rms computation. Thus:

$$I_4 = Avg.\left[I_1^2/I_4\right] = I_1\ rms$$



NOTE: PINOUTS ARE FOR 14-PIN DIP

Figure 9. Simplified Schematic

The current mirror also produces the output current, I_{OUT}, which equals $2I_4$. I_{OUT} can be used directly or converted to a voltage with R2 and buffered by A4 to provide a low impedance voltage output. The transfer function of the AD536A thus results:

$$V_{OUT} = 2R2\ I\ rms = V_{IN}\ rms$$

The dB output is derived from the emitter of Q3, since the voltage at this point is proportional to $-\log V_{IN}$. Emitter follower, Q5, buffers and level shifts this voltage, so that the dB output voltage is zero when the externally supplied emitter current (I_{REF}) to Q5 approximates I_3.

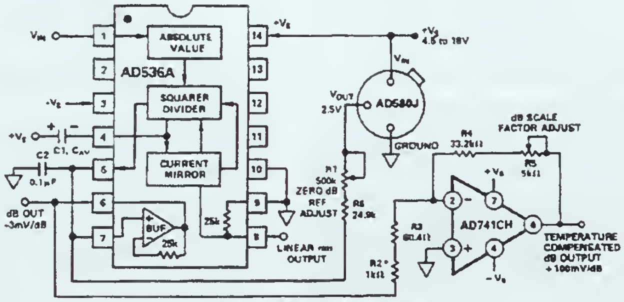
CONNECTIONS FOR dB OPERATION

A powerful feature added to the AD536A is the logarithmic or decibel output. The internal circuit computing dB works accurately over a 60 dB range. The connections for dB measurements are shown in Figure 10. The user selects the 0 dB level by adjusting R1, for the proper 0 dB reference current (which is set to exactly cancel the log output current from the squarer-divider at the desired 0 dB point). The external op amp is used to provide a more convenient scale and to allow compensation of the +0.33%/°C scale factor drift of the dB output pin. The special T.C. resistor, R2, is available from Tel Labs in Londonderry, N.H. (model Q-81) or from Precision Resistor Inc., Hillside, N.J. (model PT146). The averaged temperature coefficients of resistors R2 and R3 develop the +3300 ppm needed to reverse compensate the dB output. The linear rms output is available at Pin 8 on DIP or Pin 10 on header device with an output impedance of 25 kΩ; thus some applications may require an additional buffer amplifier if this output is desired.

dB Calibration:

1. Set V_{IN} = 1.00 V dc or 1.00 V rms
2. Adjust R1 for dB out = 0.00 V
3. Set V_{IN} = +0.1 V dc or 0.10 V rms
4. Adjust R5 for dB out = −2.00 V

Any other desired 0 dB reference level can be used by setting V_{IN} and adjusting R1, accordingly. Note that adjusting R5 for the proper gain automatically gives the correct temperature compensation.



*SPECIAL TC COMPENSATION RESISTOR +3500ppm 1% TEL LABS Q-81

Figure 10. dB Connection

FREQUENCY RESPONSE

The AD536A utilizes a logarithmic circuit in performing the implicit rms computation. As with any log circuit, bandwidth is proportional to signal level. The solid lines in the graph below represent the frequency response of the AD536A at input levels from 10 millivolts to 7 volts rms. The dashed lines indicate the upper frequency limits for 1%, 10%, and 3 dB of reading additional error. For example, note that a 1 volt rms signal will produce less than 1% of reading additional error up to 120 kHz. A 10 millivolt signal can be measured with 1% of reading additional error (100 µV) up to only 5 kHz.

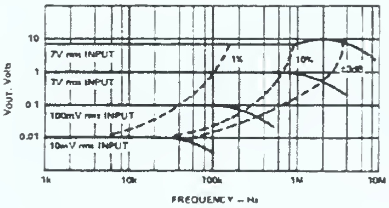


Figure 11. High Frequency Response

AC MEASUREMENT ACCURACY AND CREST FACTOR

Crest factor is often overlooked in determining the accuracy of an ac measurement. Crest factor is defined as the ratio of the peak signal amplitude to the rms value of the signal ($CF = V_P/V\ rms$). Most common waveforms, such as sine and triangle waves, have relatively low crest factors (<2). Waveforms which resemble low duty cycle pulse trains, such as those occurring in switching power supplies and SCR circuits, have high crest factors. For example, a rectangular pulse train with a 1% duty cycle has a crest factor of 10 ($CF = 1\sqrt{\eta}$).

Figure 12 is a curve of reading error for the AD536A for a 1 volt rms input signal with crest factors from 1 to 11. A rectangular pulse train (pulse width 100 µs) was used for this test since it is the worst-case waveform for rms measurement (all the energy is contained in the peaks). The duty cycle and peak amplitude were varied to produce crest factors from 1 to 11 while maintaining a constant 1 volt rms input amplitude.

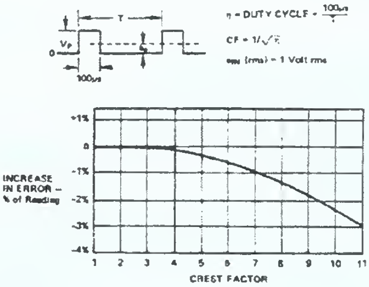


Figure 12. Error vs. Crest Factor

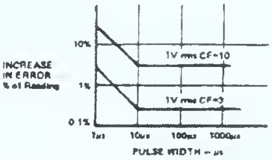


Figure 13. AD536A Error vs. Pulse Width Rectangular Pulse

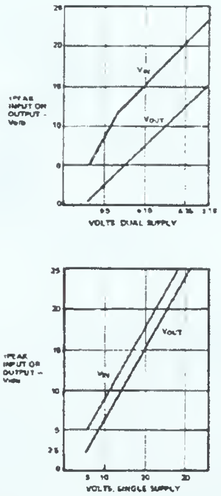
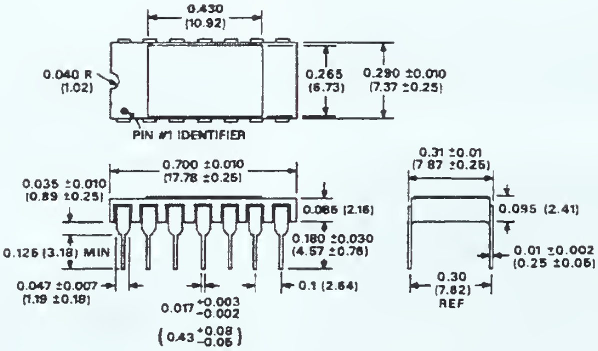


Figure 14. AD536A Input and Output Voltage Ranges vs. Supply

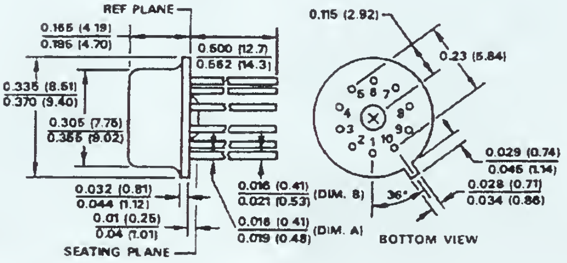
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

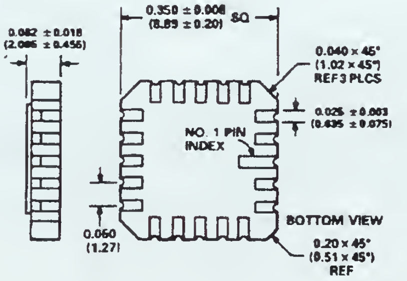
D-14 Package
TO-116



H-10A Package
TO-100



E-20A Package
LCC



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B. AD534 INTERNALLY TRIMMED PRECISION IC MULTIPLIER

ANALOG DEVICES

Internally Trimmed Precision IC Multiplier

AD534

FEATURES

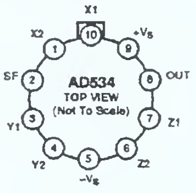
- Pretrimmed to ±0.25% max 4-Quadrant Error (AD534L)
- All Inputs (X, Y and Z) Differential, High Impedance for $[(X_1 - X_2)(Y_1 - Y_2)/10\ V] + Z_2$ Transfer Function
- Scale-Factor Adjustable to Provide up to X100 Gain
- Low Noise Design: 90 µV rms, 10 Hz–10 kHz
- Low Cost, Monolithic Construction
- Excellent Long Term Stability

APPLICATIONS

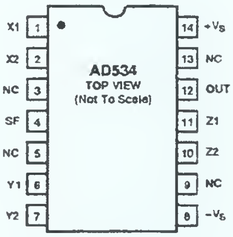
- High Quality Analog Signal Processing
- Differential Ratio and Percentage Computations
- Algebraic and Trigonometric Function Synthesis
- Wideband, High-Crest rms-to-dc Conversion
- Accurate Voltage Controlled Oscillators and Filters
- Available in Chip Form

PIN CONFIGURATIONS

TO-100 (H-10A)
Package

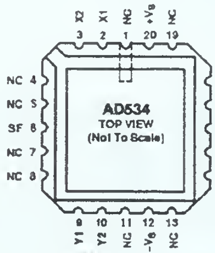


TO-116 (D-14)
Package



NC = NO CONNECT

LCC (E-20A)
Package



NC = NO CONNECT

PRODUCT DESCRIPTION

The AD534 is a monolithic laser trimmed four-quadrant multiplier divider having accuracy specifications previously found only in expensive hybrid or modular products. A maximum multiplication error of ±0.25% is guaranteed for the AD534L without any external trimming. Excellent supply rejection, low temperature coefficients and long term stability of the on-chip thin film resistors and buried Zener reference preserve accuracy even under adverse conditions of use. It is the first multiplier to offer fully differential, high impedance operation on all inputs, including the Z-input, a feature which greatly increases its flexibility and ease of use. The scale factor is pretrimmed to the standard value of 10.00 V; by means of an external resistor, this can be reduced to values as low as 3 V.

The wide spectrum of applications and the availability of several grades commend this multiplier as the first choice for all new designs. The AD534J (±1% max error), AD534K (±0.5% max) and AD534L (±0.25% max) are specified for operation over the 0°C to +70°C temperature range. The AD534S (±1% max) and AD534T (±0.5% max) are specified over the extended temperature range, –55°C to +125°C. All grades are available in hermetically sealed TO-100 metal cans and TO-116 ceramic DIP packages. AD534J, K, S and T chips are also available.

PROVIDES GAIN WITH LOW NOISE

The AD534 is the first general purpose multiplier capable of providing gains up to X100, frequently eliminating the need for separate instrumentation amplifiers to precondition the inputs. The AD534 can be very effectively employed as a variable gain differential input amplifier with high common-mode rejection. The gain option is available in all modes, and will be found to simplify the implementation of many function-fitting algorithms such as those used to generate sine and tangent. The utility of this feature is enhanced by the inherent low noise of the AD534: 90 µV, rms (depending on the gain), a factor of 10 lower than previous monolithic multipliers. Drift and feedthrough are also substantially reduced over earlier designs.

UNPRECEDENTED FLEXIBILITY

The precise calibration and differential Z-input provide a degree of flexibility found in no other currently available multiplier. Standard MDSSR functions (multiplication, division, squaring, square-rooting) are easily implemented while the restriction to particular input/output polarities imposed by earlier designs has been eliminated. Signals may be summed into the output, with or without gain and with either a positive or negative sense. Many new modes based on implicit-function synthesis have been made possible, usually requiring only external passive components. The output can be in the form of a current, if desired, facilitating such operations as integration.

REV. A

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Tel: 617/329-4700 Fax: 617/326-8703

AD534—SPECIFICATIONS (@ $T_A = +25°C$, $\pm V_S = 15$ V, $R \geq 2$ kΩ)

Model	AD534J			AD534K			AD534L			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
MULTIPLIER PERFORMANCE										
Transfer Function		$\frac{(X_1-X_2)(Y_1-Y_2)}{10\,V}+Z_2$			$\frac{(X_1-X_2)(Y_1-Y_2)}{10\,V}+Z_2$			$\frac{(X_1-X_2)(Y_1-Y_2)}{10\,V}+Z_2$		
Total Error[1] (−10 V ≤ X, Y ≤ +10 V)			**±1.0**			**±0.5**			**±0.25**	%
T_A = min to max		±1.5			±1.0			±0.5		%
Total Error vs. Temperature		±0.022			±0.015			±0.008		%/°C
Scale Factor Error (SF = 10.000 V Nominal)[2]		±0.25			±0.1			±0.1		%
Temperature-Coefficient of Scaling Voltage		±0.02			±0.01			±0.005		%/°C
Supply Rejection (±15 V ± 1 V)		±0.01			±0.01			±0.01		%
Nonlinearity, X (X = 20 V p-p, Y = 10 V)		±0.4			±0.2	**±0.3**		±0.10	**±0.12**	%
Nonlinearity, Y (Y = 20 V p-p, X = 10 V)		±0.2			±0.1	**±0.1**		±0.005	**±0.1**	%
Feedthrough[3], X (Y Nulled, X = 20 V p-p 50 Hz)		±0.3			±0.15	**±0.3**		±0.05	**±0.12**	%
Feedthrough[3], Y (X Nulled, Y = 20 V p-p 50 Hz)		±0.01			±0.01	**±0.1**		±0.005	**±0.1**	%
Output Offset Voltage		±5	**±30**		±2	**±15**		±2	**±10**	mV
Output Offset Voltage Drift		200			100			100		μV/°C
DYNAMICS										
Small Signal BW (V_{OUT} = 0.1 rms)		1			1			1		MHz
1% Amplitude Error (C_{LOAD} = 1000 pF)		50			50			50		kHz
Slew Rate (V_{OUT} 20 p-p)		20			20			20		V/μs
Settling Time (to 1%, ΔV_{OUT} = 20 V)		2			2			2		μs
NOISE										
Noise Spectral-Density SF = 10 V		0.8			0.8			0.8		μV/√Hz
SF = 3 V[4]		0.4			0.4			0.4		μV/√Hz
Wideband Noise f = 10 Hz to 5 MHz		1			1			1		mV/rms
f = 10 Hz to 10 kHz		90			90			90		μV/rms
OUTPUT										
Output Voltage Swing	**±11**			**±11**			**±11**			V
Output Impedance (f ≤ 1 kHz)		0.1			0.1			0.1		Ω
Output Short Circuit Current (R_L = 0, T_A = min to max)		30			30			30		mA
Amplifier Open Loop Gain (f = 50 Hz)		70			70			70		dB
INPUT AMPLIFIERS (X, Y and Z)[5]										
Signal Voltage Range (Diff. or CM		±10			±10			±10		V
Operating Diff.)		±12			±12			±12		V
Offset Voltage X, Y		±5	**±20**		±2	**±10**		±2	**±10**	mV
Offset Voltage Drift X, Y		100			50			50		μV/°C
Offset Voltage Z		±5	**±30**		±2	**±15**		±2	**±10**	mV
Offset Voltage Drift Z		200			100			100		μV/°C
CMRR	**60**	80		**70**	90		**70**	90		dB
Bias Current		0.8	**2.0**		0.8	**2.0**		0.8	**2.0**	μA
Offset Current		0.1			0.1			0.05	**0.2**	μA
Differential Resistance		10			10			10		MΩ
DIVIDER PERFORMANCE										
Transfer Function ($X_1 > X_2$)		$10\,V\frac{(Z_2-Z_1)}{(X_1-X_2)}+Y_1$			$10\,V\frac{(Z_2-Z_1)}{(X_1-X_2)}+Y_1$			$10\,V\frac{(Z_2-Z_1)}{(X_1-X_2)}+Y_1$		
Total Error[1] (X = 10 V, −10 V ≤ Z ≤ +10 V)		±0.75			±0.35			±0.2		%
(X = 1 V, −1 V ≤ Z ≤ +1 V)		±2.0			±1.0			±0.8		%
(0.1 V ≤ X ≤ 10 V, −10 V ≤ Z ≤ 10 V)		±2.5			±1.0			±0.8		%
SQUARE PERFORMANCE										
Transfer Function		$\frac{(X_1-X_2)^2}{10\,V}+Z_2$			$\frac{(X_1-X_2)^2}{10\,V}+Z_2$			$\frac{(X_1-X_2)^2}{10\,V}+Z_2$		
Total Error (−10 V ≤ X ≤ 10 V)		±0.6			±0.3			±0.2		%
SQUARE-ROOTER PERFORMANCE										
Transfer Function ($Z_1 \leq Z_2$)		$\sqrt{10\,V(Z_2-Z_1)}+X_2$			$\sqrt{10\,V(Z_2-Z_1)}+X_2$			$\sqrt{10\,V(Z_2-Z_1)}+X_2$		
Total Error[1] (1 V ≤ Z ≤ 10 V)		±1.0			±0.5			±0.25		%
POWER SUPPLY SPECIFICATIONS										
Supply Voltage										
Rated Performance		±15			±15			±15		V
Operating	**±8**		**±18**	**±8**		**±18**	**±8**		**±18**	V
Supply Current										
Quiescent		4	**6**		4	**6**		4	**6**	mA
PACKAGE OPTIONS										
TO-100 (H-10A)		AD534JH			AD534KH			AD534LH		
TO-116 (D-14)		AD534JD			AD534KD			AD534LD		
Chips		AD534J Chips			AD534K Chips					

NOTES

[1] Figures given are percent of full scale, ±10 V (i.e., 0.01% = 1 mV).
[2] May be reduced down to 3 V using external resistor between $-V_S$ and SF.
[3] Irreducible component due to nonlinearity: excludes effect of offsets.
[4] Using external resistor adjusted to give SF = 3 V.
[5] See Functional Block Diagram for definition of sections.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Model	AD534S			AD534T			Units
	Min	Typ	Max	Min	Typ	Max	
MULTIPLIER PERFORMANCE							
Transfer Function		$\frac{(X_1 - X_2)(Y_1 - Y_2)}{10\,V} + Z_2$			$\frac{(X_1 - X_2)(Y_1 - Y_2)}{10\,V} + Z_2$		
Total Error[1] (−10 V ≤ X, Y ≤ +10 V)			**±1.0**			**±0.5**	%
T_A = min to max			**±2.0**		±1.0		%
Total Error vs. Temperature			**±0.02**			**±0.01**	%/°C
Scale Factor Error (SF = 10.000 V Nominal)[2]		±0.25			±0.1		%
Temperature-Coefficient of Scaling Voltage		±0.02				**±0.005**	%/°C
Supply Rejection (±15 V ± 1 V)		±0.01			±0.01		%
Nonlinearity, X (X = 20 V p-p, Y = 10 V)		±0.4			±0.2	**±0.3**	%
Nonlinearity, Y (Y = 20 V p-p, X = 10 V)		±0.2			±0.1	**±0.1**	%
Feedthrough[3], X (Y Nulled, X = 20 V p-p 50 Hz)		±0.3			±0.15	**±0.3**	%
Feedthrough[3], Y (X Nulled, Y = 20 V p-p 50 Hz)		±0.01			±0.01	**±0.1**	%
Output Offset Voltage		±5	**±30**		±2	**±15**	mV
Output Offset Voltage Drift			**500**			**300**	µV/°C
DYNAMICS							
Small Signal BW (V_{OUT} = 0.1 rms)		1			1		MHz
1% Amplitude Error (C_{LOAD} = 1000 pF)		50			50		kHz
Slew Rate (V_{OUT} 20 p-p)		20			20		V/µs
Settling Time (to 1%, ΔV_{OUT} = 20 V)		2			2		µs
NOISE							
Noise Spectral-Density SF = 10 V		0.8			0.8		µV/√Hz
SF = 3 V[4]		0.4			0.4		µV/√Hz
Wideband Noise f = 10 Hz to 5 MHz		1.0			1.0		mV/rms
f = 10 Hz to 10 kHz		90			90		µV/rms
OUTPUT							
Output Voltage Swing	**±11**			**±11**			V
Output Impedance (f ≤ 1 kHz)		0.1			0.1		Ω
Output Short Circuit Current (R_L = 0, T_A = min to max)		30			30		mA
Amplifier Open Loop Gain (f = 50 Hz)		70			70		dB
INPUT AMPLIFIERS (X, Y and Z)[5]							
Signal Voltage Range (Diff. or CM		±10			±10		V
Operating Diff.)		±12			±12		V
Offset Voltage X, Y		±5	**±20**		±2	**±10**	mV
Offset Voltage Drift X, Y		100			150		µV/°C
Offset Voltage Z		±5	**±30**		±2	**±15**	mV
Offset Voltage Drift Z			**500**			**300**	µV/°C
CMRR	**60**	80		**70**	90		dB
Bias Current		0.8	**2.0**		0.8	**2.0**	µA
Offset Current		0.1			0.1		µA
Differential Resistance		10			10		MΩ
DIVIDER PERFORMANCE							
Transfer Function ($X_1 > X_2$)		$10\,V \frac{(Z_2 - Z_1)}{(X_1 - X_2)} + Y_1$			$10\,V \frac{(Z_2 - Z_1)}{(X_1 - X_2)} + Y_1$		
Total Error[1] (X = 10 V, −10 V ≤ Z ≤ +10 V)		±0.75			±0.35		%
(X = 1 V, −1 V ≤ Z ≤ +1 V)		±2.0			±1.0		%
(0.1 V ≤ X ≤ 10 V, −10 V ≤ Z ≤ 10 V)		±2.5			±1.0		%
SQUARE PERFORMANCE							
Transfer Function		$\frac{(X_1 - X_2)^2}{10\,V} + Z_2$			$\frac{(X_1 - X_2)^2}{10\,V} + Z_2$		
Total Error (−10 V ≤ X ≤ 10 V)		±0.6			±0.3		%
SQUARE-ROOTER PERFORMANCE							
Transfer Function ($Z_1 \le Z_2$)		$\sqrt{10\,V(Z_2 - Z_1)} + X_2$			$\sqrt{10\,V(Z_2 - Z_1)} + X_2$		
Total Error[1] (1 V ≤ Z ≤ 10 V)		±1.0			±0.5		%
POWER SUPPLY SPECIFICATIONS							
Supply Voltage							
Rated Performance		±15			±15		V
Operating	**±8**		**±22**	**±8**		**±22**	V
Supply Current							
Quiescent		4	**6**		4	**6**	mA
PACKAGE OPTIONS							
TO-100 (H-10A)		AD534SH			AD534TH		
TO-116 (D-14)		AD534SD			AD534TD		
E-20A		AD534SE			AD534TE		
Chips		AD534S Chips			AD534T Chips		

NOTES

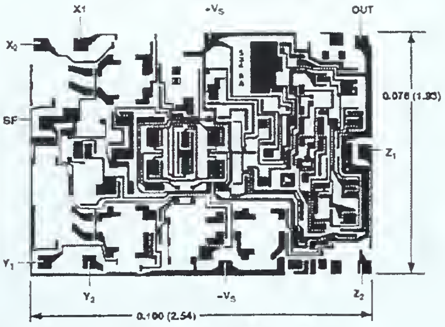
[1] Figures given are percent of full scale, ±10 V (i.e., 0.01% = 1 mV).
[2] May be reduced down to 3 V using external resistor between $-V_S$ and SF.
[3] Irreducible component due to nonlinearity: excludes effect of offsets.
[4] Using external resistor adjusted to give SF = 3 V.
[5] See Functional Block Diagram for definition of sections.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

CHIP DIMENSIONS AND BONDING DIAGRAM

Dimensions shown in inches and (mm).
Contact factory for latest dimensions.



THE AD534 IS AVAILABLE IN LASER - TRIMMED CHIP FORM

Thermal Characteristics

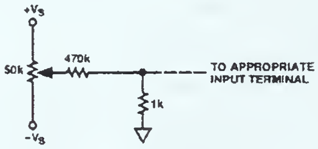
Thermal Resistance θ_{JC} = 25°C/W for H-10A
θ_{JA} = 150°C/W for H-10A
θ_{JC} = 25°C/W for D-14 or E-20A
θ_{JA} = 95°C/W for D-14 or E-20A

ABSOLUTE MAXIMUM RATINGS

	AD534J, K, L	AD534S, T
Supply Voltage	±18 V	±22 V
Internal Power Dissipation	500 mW	*
Output Short-Circuit to Ground	Indefinite	*
Input Voltages, X_1 X_2 Y_1 Y_2 Z_1 Z_2	$\pm V_S$	*
Rated Operating Temperature Range	0°C to +70°C	–55°C to +125°C
Storage Temperature Range	–65°C to +150°C	*
Lead Temperature Range, 60 s Soldering	+300°C	*

*Same as AD534J Specs.

OPTIONAL TRIMMING CONFIGURATION



ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD534JD	0°C to +70°C	Side Brazed DIP	D-14
AD534KD	0°C to +70°C	Side Brazed DIP	D-14
AD534LD	0°C to +70°C	Side Brazed DIP	D-14
AD534JH	0°C to +70°C	Header	H-10A
AD534KH	0°C to +70°C	Header	H-10A
AD534LH	0°C to +70°C	Header	H-10A
AD534J Chip	0°C to +70°C	Chip	
AD534K Chip	0°C to +70°C	Chip	
AD534SD	–55°C to +125°C	Side Brazed DIP	D-14
AD534SD/883B	–55°C to +125°C	Side Brazed DIP	D-14
AD534TD	–55°C to +125°C	Side Brazed DIP	D-14
AD534TD/883B	–55°C to +125°C	Side Brazed DIP	D-14
JM38510/13902BCA	–55°C to +125°C	Side Brazed DIP	D-14
JM38510/13901BCA	–55°C to +125°C	Side Brazed DIP	D-14
AD534SE	–55°C to +125°C	LCC	E-20A
AD534SE/883B	–55°C to +125°C	LCC	E-20A
AD534TE	–55°C to +125°C	LCC	E-20A
AD534TE/883B	–55°C to +125°C	LCC	E-20A
AD534SH	–55°C to +125°C	Header	H-10A
AD534SH/883B	–55°C to +125°C	Header	H-10A
AD534TH	–55°C to +125°C	Header	H-10A
AD534TH/883B	–55°C to +125°C	Header	H-10A
JM38510/13902BIA	–55°C to +125°C	Header	H-10A
JM38510/13901BIA	–55°C to +125°C	Header	H-10A
AD534S Chip	–55°C to +125°C	Chip	
AD534T Chip	–55°C to +125°C	Chip	

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD534 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

WARNING!
ESD SENSITIVE DEVICE

FUNCTIONAL DESCRIPTION

Figure 1 is a functional block diagram of the AD534. Inputs are converted to differential currents by three identical voltage-to-current converters, each trimmed for zero offset. The product of the X and Y currents is generated by a multiplier cell using Gilbert's translinear technique. An on-chip "Buried Zener" provides a highly stable reference, which is laser trimmed to provide an overall scale factor of 10 V. The difference between XY/SF and Z is then applied to the high gain output amplifier. This permits various closed loop configurations and dramatically reduces nonlinearities due to the input amplifiers, a dominant source of distortion in earlier designs. The effectiveness of the new scheme can be judged from the fact that under typical conditions as a multiplier the nonlinearity on the Y input, with X at full scale (±10 V), is ±0.005% of F.S.; even at its worst point, which occurs when X = ±6.4 V, it is typically only ±0.05% of F.S. Nonlinearity for signals applied to the X input, on the other hand, is determined almost entirely by the multiplier element and is parabolic in form. This error is a major factor in determining the overall accuracy of the unit and hence is closely related to the device grade.

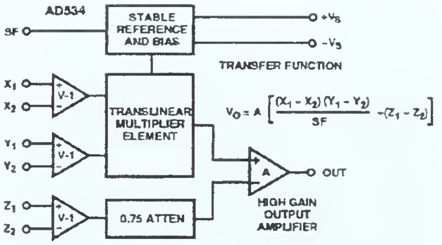

AD534
SF
STABLE REFERENCE AND BIAS
+V_S
-V_S
TRANSFER FUNCTION
X₁
X₂
V-1
Y₁
Y₂
V-1
TRANSLINEAR MULTIPLIER ELEMENT
V_O = A [(X₁ - X₂) (Y₁ - Y₂) / SF - (Z₁ - Z₂)]
A
OUT
Z₁
Z₂
V-1
0.75 ATTEN
HIGH GAIN OUTPUT AMPLIFIER

Figure 1. AD534 Functional Block Diagram

The generalized transfer function for the AD534 is given by:

$$V_{OUT} = A\left(\frac{(X_1 - X_2)(Y_1 - Y_2)}{SF} - (Z_1 - Z_2)\right)$$

where A = open loop gain of output amplifier, typically 70 dB at dc

X, Y, Z = input voltages (full scale = ±SF, peak = ±1.25 SF)

SF = scale factor, pretrimmed to 10.00 V but adjustable by the user down to 3 V.

In most cases the open loop gain can be regarded as infinite, and SF will be 10 V. The operation performed by the AD534, can then be described in terms of equation:

$$(X_1 - X_2)(Y_1 - Y_2) = 10\,V\,(Z_1 - Z_2)$$

The user may adjust SF for values between 10.00 V and 3 V by connecting an external resistor in series with a potentiometer between SF and $-V_S$. The approximate value of the total resistance for a given value of SF is given by the relationship:

$$R_{SF} = 5.4K\,\frac{SF}{10 - SF}$$

Due to device tolerances, allowance should be made to vary R_{SF} by ±25% using the potentiometer. Considerable reduction in bias currents, noise and drift can be achieved by decreasing SF. This has the overall effect of increasing signal gain without the customary increase in noise. Note that the peak input signal is always limited to 1.25 SF (i.e., ±5 V for SF = 4 V) so the overall transfer function will show a maximum gain of 1.25. The performance with small input signals, however, is improved by using a lower SF since the dynamic range of the inputs is now fully utilized. Bandwidth is unaffected by the use of this option.

Supply voltages of ±15 V are generally assumed. However, satisfactory operation is possible down to ±8 V (see curve 1). Since all inputs maintain a constant peak input capability of ±1.25 SF some feedback attenuation will be necessary to achieve output voltage swings in excess of ±12 V when using higher supply voltages.

OPERATION AS A MULTIPLIER

Figure 2 shows the basic connection for multiplication. Note that the circuit will meet all specifications without trimming.

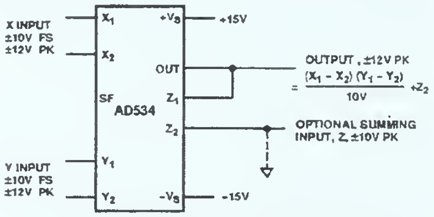


Figure 2. Basic Multiplier Connection

In some cases the user may wish to reduce ac feedthrough to a minimum (as in a suppressed carrier modulator) by applying an external trim voltage (±30 mV range required) to the X or Y input (see Optional Trimming Configuration, page 3). Curve 4 shows the typical ac feedthrough with this adjustment mode. Note that the Y input is a factor of 10 lower than the X input and should be used in applications where null suppression is critical.

The high impedance Z_2 terminal of the AD534 may be used to sum an additional signal into the output. In this mode the output amplifier behaves as a voltage follower with a 1 MHz small signal bandwidth and a 20 V/µs slew rate. This terminal should always be referenced to the ground point of the driven system, particularly if this is remote. Likewise the differential inputs should be referenced to their respective ground potentials to realize the full accuracy of the AD534.

A much lower scaling voltage can be achieved without any reduction of input signal range using a feedback attenuator as shown in Figure 3. In this example, the scale is such that $V_{OUT} = XY$, so that the circuit can exhibit a maximum gain of 10. This connection results in a reduction of bandwidth to about 80 kHz without the peaking capacitor C_F = 200 pF. In addition, the output offset voltage is increased by a factor of 10 making external adjustments necessary in some applications. Adjustment is made by connecting a 4.7 MΩ resistor between Z_1 and the slider of a pot connected across the supplies to provide ±300 mV of trim range at the output.

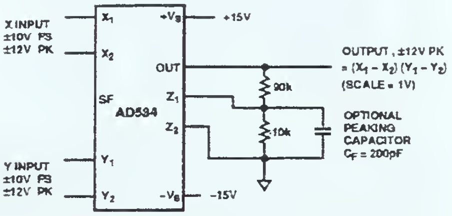


Figure 3. Connections for Scale-Factor of Unity

Feedback attenuation also retains the capability for adding a signal to the output. Signals may be applied to the high impedance Z_2 terminal where they are amplified by +10 or to the common ground connection where they are amplified by +1. Input signals may also be applied to the lower end of the 10 kΩ resistor, giving a gain of −9. Other values of feedback ratio, up to X100, can be used to combine multiplication with gain.

Occasionally it may be desirable to convert the output to a current, into a load of unspecified impedance or dc level. For example, the function of multiplication is sometimes followed by integration; if the output is in the form of a current, a simple capacitor will provide the integration function. Figure 4 shows how this can be achieved. This method can also be applied in squaring, dividing and square rooting modes by appropriate choice of terminals. This technique is used in the voltage-controlled low-pass filter and the differential-input voltage-to-frequency converter shown in the Applications Section.

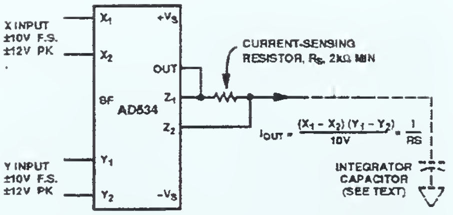


Figure 4 Conversion of Output to Current

OPERATION AS A SQUARER

Operation as a squarer is achieved in the same fashion as the multiplier except that the X and Y inputs are used in parallel. The differential inputs can be used to determine the output polarity (positive for $X_1 = Y_1$ and $X_2 = Y_2$, negative if either one of the inputs is reversed). Accuracy in the squaring mode is typically a factor of 2 better than in the multiplying mode, the largest errors occurring with small values of output for input below 1 V.

If the application depends on accurate operation for inputs that are always less than ±3 V, the use of a reduced value of SF is recommended as described in the FUNCTIONAL DESCRIPTION section (previous page). Alternatively, a feedback attenuator may be used to raise the output level. This is put to use in the difference-of-squares application to compensate for the factor of 2 loss involved in generating the sum term (see Figure 7).

The difference-of-squares function is also used as the basis for a novel rms-to-dc converter shown in Figure 14. The averaging filter is a true integrator, and the loop seeks to zero its input. For this to occur, $(V_{IN})^2 - (V_{OUT})^2 = 0$ (for signals whose period is well below the averaging time-constant) Hence V_{OUT} is forced to equal the rms value of V_{IN}. The absolute accuracy of this technique is very high; at medium frequencies, and for signals near full scale, it is determined almost entirely by the ratio of the resistors in the inverting amplifier. The multiplier scaling voltage affects only open loop gain. The data shown is typical of performance that can be achieved with an AD534K, but even using an AD534J, this technique can readily provide better than 1% accuracy over a wide frequency range, even for crest-factors in excess of 10.

OPERATION AS A DIVIDER

The AD535, a pin for pin functional equivalent to the AD534, has guaranteed performance in the divider and square-rooter configurations and is recommended for such applications.

Figure 5 shows the connection required for division. Unlike earlier products, the AD534 provides differential operation on both numerator and denominator, allowing the ratio of two floating variables to be generated. Further flexibility results from access to a high impedance summing input to Y_1. As with all dividers based on the use of a multiplier in a feedback loop, the bandwidth is proportional to the denominator magnitude, as shown in curve 8.

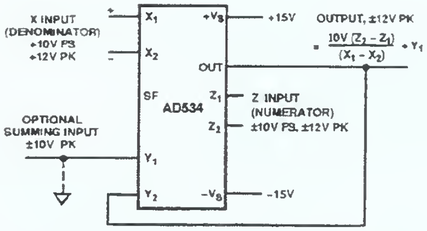

X INPUT (DENOMINATOR) +10V FS +12V PK
+
−
X_1
X_2
SF
AD534
Y_1
Y_2
$+V_S$
OUT
Z_1
Z_2
$-V_S$
+15V
−15V
OUTPUT, ±12V PK
$= \frac{10V(Z_2 - Z_1)}{(X_1 - X_2)} + Y_1$
Z INPUT (NUMERATOR) ±10V FS, ±12V PK
OPTIONAL SUMMING INPUT ±10V PK

Figure 5. Basic Divider Connection

Without additional trimming, the accuracy of the AD534K and L is sufficient to maintain a 1% error over a 10 V to 1 V denominator range. This range may be extended to 100:1 by simply reducing the X offset with an externally generated trim voltage (range required is ±3.5 mV max) applied to the unused X input (see Optional Trimming Configuration). To trim, apply a ramp of +100 mV to +V at 100 Hz to both X_1 and Z_2 (if X_2 is used for offset adjustment, otherwise reverse the signal polarity) and adjust the trim voltage to minimize the variation in the output.*

Since the output will be near +10 V, it should be ac-coupled for this adjustment. The increase in noise level and reduction in bandwidth preclude operation much beyond a ratio of 100 to 1.

As with the multiplier connection, overall gain can be introduced by inserting a simple attenuator between the output and Y_2 terminal. This option, and the differential-ratio capability of the AD534 are utilized in the percentage-computer application shown in Figure 11. This configuration generates an output proportional to the percentage deviation of one variable (A) with respect to a reference variable (B), with a scale of one volt per percent

OPERATION AS A SQUARE ROOTER

The operation of the AD534 in the square root mode is shown in Figure 6. The diode prevents a latching condition which could occur if the input momentarily changes polarity. As shown, the output is always positive; it may be changed to a negative output by reversing the diode direction and interchanging the X inputs. Since the signal input is differential, all combinations of input and output polarities can be realized, but operation is restricted to the one quadrant associated with each combination of inputs

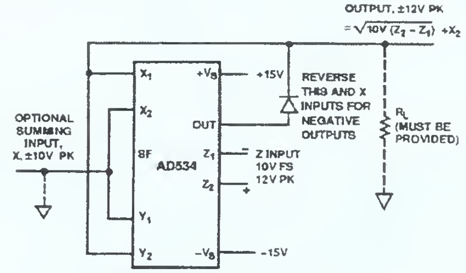


Figure 6. Square-Rooter Connection

In contrast to earlier devices, which were intolerant of capacitive loads in the square root modes, the AD534 is stable with all loads up to at least 1000 pF. For critical applications, a small adjustment to the Z input offset (see Optional Trimming Configuration) will improve accuracy for inputs below 1 V.

*See the AD535 Data Sheet for more details.

AD534–Applications Section

The versatility of the AD534 allows the creative designer to implement a variety of circuits such as wattmeters, frequency doublers and automatic gain controls to name but a few.

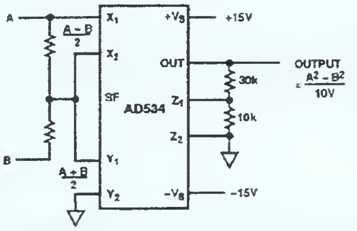
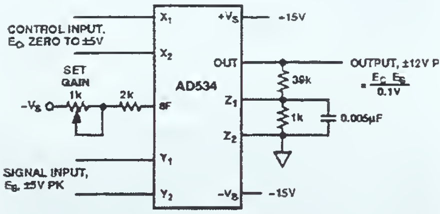


Figure 7. Difference-of-Squares



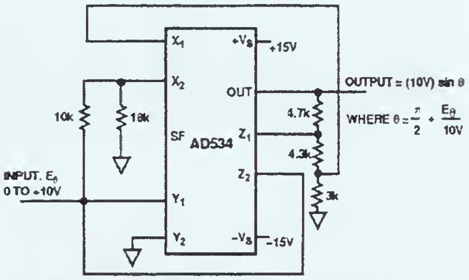
NOTES: 1) GAIN IS X 10 PER-VOLT OF E_C, ZERO TO X 50

2) WIDEBAND (10Hz – 30kHz) OUTPUT NOISE IS 3mV RMS, TYP CORRESPONDING TO A F.S. S/N RATIO OF 70dB

3) NOISE REFERED TO SIGNAL INPUT, WITH E_C = ±5V, IS 60µV RMS, TYP

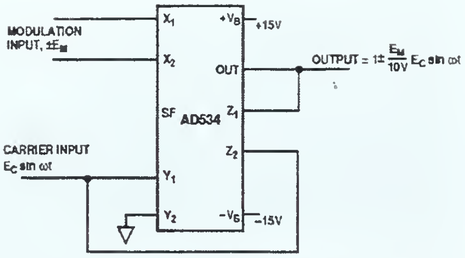
4) BANDWITH IS DC TO 20kHz, −3dB, INDEPENDENT OF GAIN

Figure 8. Voltage-Controlled Amplifier



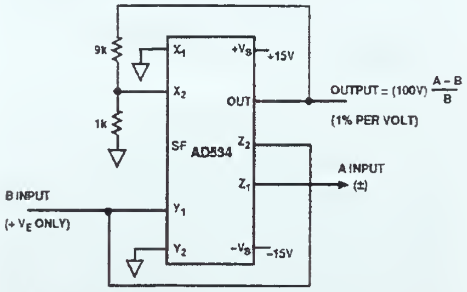
USING CLOSE TOLERANCE RESISTORS AND AD534L, ACCURACY OF FIT IS WITHIN ±0.5% AT ALL POINTS. θ IS IN RADIANS.

Figure 9. Sine-Function Generator


MODULATION INPUT, $\pm E_M$
CARRIER INPUT E_C sin ωt
X_1
X_2
SF
Y_1
Y_2
AD534
$+V_S$
OUT
Z_1
Z_2
$-V_S$
+15V
−15V
OUTPUT = $1 \pm \frac{E_M}{10V} E_C$ sin ωt

THE SF PIN OR A Z-ATTENUATOR CAN BE USED TO PROVIDE OVERALL SIGNAL AMPLIFICATION, OPERATION FROM A SINGLE SUPPLY POSSIBLE: BIAS Y_2 TO $V_S/2$.

Figure 10. Linear AM Modulator



OTHER SCALES, FROM 10% PER VOLT TO 0.1% PER VOLT CAN BE OBTAINED BY ALTERING THE FEEDBACK RATIO.

Figure 11. Percentage Computer

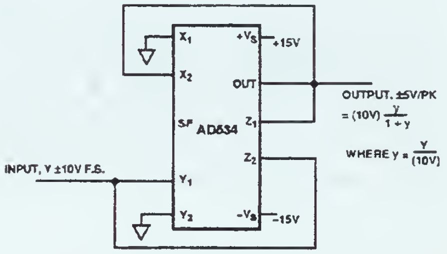
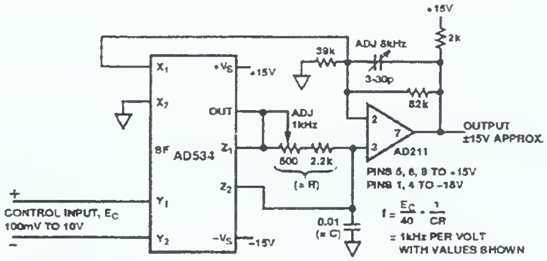


Figure 12. Bridge-Linearization Function



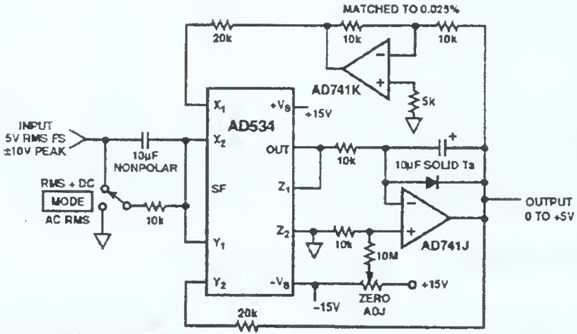
CALIBRATION PROCEDURE:

WITH E_C = 1.0V, ADJUST POT TO SET f = 1.000kHz. WITH E_C = 8.0V ADJUST TRIMMER CAPACITOR TO SET f = 8.000kHz. LINEARITY WILL TYPICALLY BE WITHIN ± 0.1% OF F.S. FOR ANY OTHER INPUT.

DUE TO DELAYS IN THE COMPARATOR, THIS TECHNIQUE IS NOT SUITABLE FOR MAXIMUM FREQUENCIES ABOVE 10kHz. FOR FREQUENCIES ABOVE 10kHz THE AD537 VOLTAGE TO FREQUENCY CONVERTER IS RECOMMENDED.

A TRIANGLE -WAVE OF ±5V PK APPEARS ACROSS THE 0.01µF CAPACITOR; IF USED AS AN OUTPUT, A VOLTAGE- FOLLOWER SHOULD BE INTERPOSED.

Figure 13. Differential-Input Voltage-to-Frequency Converter



CALIBRATION PROCEDURE:

WITH 'MODE' SWITCH IN 'RMS+ DC' POSITION, APPLY AN INPUT OF +1.00VDC. ADJUST ZERO UNTIL OUTPUT READS SAME AS INPUT. CHECK FOR INPUTS OF ±10V: OUTPUT SHOULD BE WITHIN ±0.05% (5mV).

ACCURACY IS MAINTAINED FROM 60Hz TO 100kHz, AND IS TYPICALLY HIGH BY 0.5% AT 1MHz FOR V_{IN} = 4V RMS (SINE, SQUARE OR TRIANGULAR-WAVE).

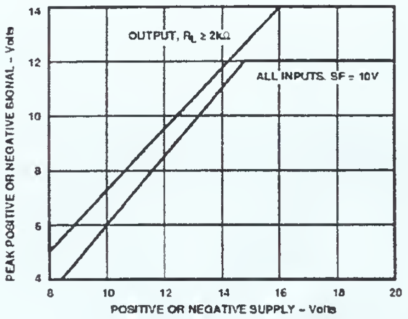
PROVIDED THAT THE PEEK INPUT IS NOT EXCEEDED, CREST-FACTORS UP TO AT LEAST TEN HAVE NO APPRECIABLE EFFECT ON ACCURACY .

INPUT IMPEDANCE IS ABOUT 10kΩ; FOR HIGH (10MΩ) IMPEDANCE REMOVE MODE SWITCH AND INPUT COUPLING COMPONENTS.

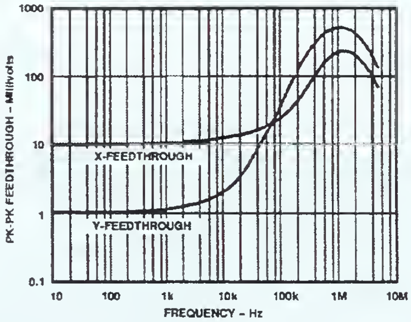
FOR GUARANTEED SPECIFICATIONS THE AD536A AND AD636 IS OFFERED AS A SINGLE PACKAGE RMS-TO-DC CONVERTER.

Figure 14. Wideband, High-Crest Factor, RMS-to-DC Converter

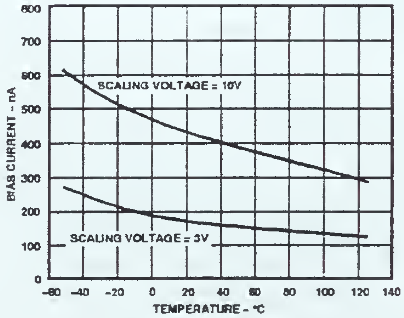
AD534—Typical Performance Curves *(typical at +25°C, with $V_S = \pm 15$ V dc, unless otherwise noted)*



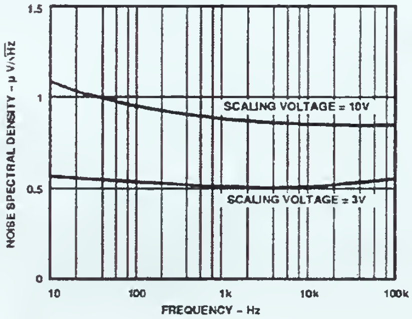
Curve 1. Input/Output Signal Range vs. Supply Voltages



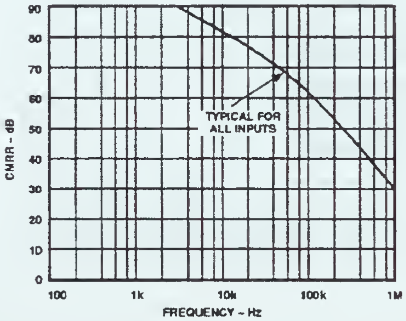
Curve 4. AC Feedthrough vs. Frequency



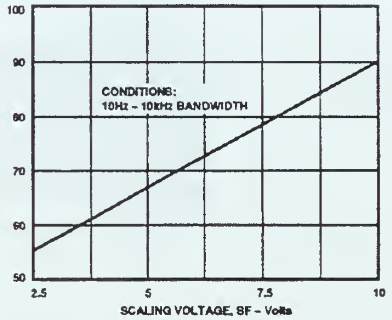
Curve 2. Bias Currents vs. Temperature (X, Y or Z Inputs)



Curve 5. Noise Spectral Density vs. Frequency



Curve 3. Common-Mode Rejection Ratio vs. Frequency



Curve 6. Wideband Noise vs. Scaling Voltage

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